Allwinner Technology

Allwinner A23 Datasheet

Dual Core Mobile Application Processor

Revision 1.0

August 30, 2013

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Revision History

Revision	Date	Description
1.0	August 30, 2013	Initial version

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1 OVERVIEW

The Allwinner A23 is a remarkably power-efficient dual-core mobile application processor based on ARM Cortex™-A7 CPU along with Mali400MP2 GPU architecture. It is also highly competitive in terms of system cost thanks to its high system integration and is capable of delivering excellent user experience while maintaining low power consumption.

Main features of A23 include:

- CPU architecture: A23 is based on dual-core Cortex™-A7 CPU architecture, the most power efficient CPU core ARM's ever developed, to deliver superior system performance as well as optimized battery life experience;
- Graphic: A23 adopts the extensively implemented and technically mature Mali400MP2 GPU to provide end users with superior experience in web browsing, video playback and games; OpenGL ES 2.0 and OpenVG 1.1 standards are supported;
- Video Engine: A23 supports high-definition 1080P video processing and various mainstream video standards such as H.264, VP8, MPEG 1/2/4, JPEG/MJPEG, etc;
- Display: A23 supports CPU/RGB/LVDS LCD interface up to 1280x800 resolution. Four-lane MIPI DSI (Display Serial Interface) is integrated as well, supporting MIPI DSI V1.01 and MIPI D-PHY V1.00;
- Image: A23 supports a parallel CMOS sensor interface up to 5M resolution

Thanks to its advanced system design and outstanding software optimization, the A23 is capable of providing top-notch system performance with long-lasting battery life experience: in addition to its energy-efficient Cortex™-A7 CPU architecture, advanced fabrication process, video acceleration hardware, DVFS technology support and high system integration, A23 also features a unique Talking Standby Mode where the processor can be inactive during voice calls to provide end users with ultra-long battery life experience. Additionally, Allwinner A23 features high system integration with a wide range of integrated I/Os like 4-lane MIPI DSI, LVDS, USB OTG/HOST, SD/MMC, I2S/PCM, thus significantly reducing system components required in design to simplify product design and reduce total system costs.

2 FEATURES

2.1. CPU Architecture

The A23 platform is based on dual-core Cortex™-A7 CPU architecture.

- ARMv7 ISA standard instruction set plus Thumb-2 and Jazeller RCT
- NEON with SIMD and VFPv4 support
- Support hardware virtualization
- Support LPAE
- Support 4GB address space
- Support 128KB L1 cache and shared 256KB L2 cache
- Support DVFS with independent power domain

2.2. GPU

- Mali400MP2 GPU
- Support OpenGL ES 2.0 / OpenVG 1.1 standard

2.3. Memory Subsystem

This section consists of:

- Boot ROM
- SDRAM
- NAND Flash
- SD/MMC interface

Boot ROM

- Support system boot from Raw NAND, eMMC NAND, SPI NOR Flash, and SD/TF card
- Support system code download through USB OTG

SDRAM

- Support 1GB address space
- Support 16-bit bus width
- Support DDR3 /DDR3L SDRAM

NAND Flash

- Comply to ONFI 2.3 and Toggle 1.0
- Support 64-bit ECC per 512 bytes or 1024 bytes
- Support 8-bit Raw NAND flash controller sharing pin with eMMC
- Support 3.0V IO voltage
- Support 2 CE and 2 RB signals
- Support SLC/MLC/TLC NAND and EF-NAND

SD/MMC Interface

- Comply to eMMC standard specification V4.41, SD physical layer specification V2.0, SDIO card specification V2.0
- Support 4/8-bit bus width
- Support HS/DS/SDR12/SDR25 bus mode
- Support 3 SD/MMC controllers
- Support SDIO interrupt detection
- Support 3.0V IO voltage

2.4. System Peripheral

This section includes:

- Timer
- High Speed Timer
- RTC
- GIC
- DMA
- CCU
- PWM

Timer

- Support two timers: clock source can be switched over 24MHz and 32768Hz
- Support two 33-bit AVS counters
- Support one 64-bit system counter from 24MHz
- Support a watchdog to generate reset signal or interrupts

High Speed Timer

- Clock source is fixed to AHB, and the pre-scale ranges from 1 to 16
- Support a 56-bit counter

RTC

- Support full clock features: second/minute/hour/day/month/year
- Support a 32768Hz clock fanout

GIC

- Support 16 SGIs, 16 PPIs and 128 SPIs
- Support ARM architecture security extensions
- Support ARM architecture virtualization extensions
- Support single processor and multiple processors environment

DMA

- 8-channel DMA
- Support data width of 8/16/32 bits
- Support linear and IO address modes

CCU

- 9 PLLs
- Support a 24MHz oscillator, a 32768Hz oscillator and an on-chip RC oscillator

PWM

- Support three PWM outputs
- Support cycle mode and pulse mode
- Support prescale from 1 to 64

2.5. Display Subsystem

This section includes:

- Display engine
- Video output

Display Engine

- Four movable layers, each layer size up to 8192x8192 pixels
- Ultra-Scaling engine
  - Support four-tap scale filter in both horizontal and vertical
  - Support source image size from 8x4 to 8192x8192 resolution and destination image size from 8x4 to 8192x8192 resolution
- Support multiple image input formats: mono 1/2/4/8bpp, palette 1/2/4/8bpp, 6/24/32bpp color, YUV444/420/422/411
- Support alpha blending / color key / gamma
- Support output color correction: luminance / hue / saturation, etc
- Support Color Management Unit (CMU) and Dynamic Range Correction (DRC)
- Support realtime write back function

Video Output

- Support CPU / Sync RGB / LVDS LCD interface up to 1280x800 resolution
- Support 1/2/4-lane MIPI DSI interface up to 1280x800 resolution
  - Support MIPI DSI V1.01 and MIPI D-PHY V1.00
  - Support command mode and video mode (non-burst mode with sync pulses, non-burst mode with sync event and burst mode)
- Support RGB666 dither function

2.6. Video Engine

Video Decoding

- Support video playback up to 1920x1080@60fps
- Support multi-format video playback, including MPEG1/2, MPEG4 SP/ASP GMC, H.263 including Sorenson Spark, H.264 BP/MP/HP, VP8, WMV9/VC-1, JPEG/MJPEG, etc

Video Encoding

- Support H.264 HP video encoding up to 1920x1080@60fps
- JPEG baseline: picture size up to 4080x4080
- Support Alpha blending
- Support thumb generation
- Support 4x2 scaling ratio: from 1/16 to 64 arbitrary non-integer ratio

2.7. Image Subsystem

CSI

- Support parallel camera sensor
- Support 8-bit CCIR601/656 interface
- Support up to 5M pixel camera sensor
- Support dual outputs for display and encoding

2.8. Audio Subsystem

Audio Codec

- Support stereo audio DAC
  - –Up to 100dB SNR
  - –8KHz ~ 192KHz DAC sample rate
- Support stereo audio ADC
  - –Up to 94dB SNR
  - –8KHz ~ 48KHz ADC sample rate
- Support four analog audio inputs
  - –Two microphone differential inputs for main mic and headphone mic
  - –One differential phone input for modem
  - –One stereo line-in input for FM
- Support two analog audio outputs
  - –One stereo or differential capless headphone output
  - –One differential earpiece output
- Support Talking Standby Mode, where the application processor remains inactive during voice call application for power saving

2.9. External Peripherals

This section includes:

- USB 2.0 OTG
- USB HOST
- LRADC
- Digital Audio Interface
- UART
- SPI
- Open-drain TWI
- RSB™

USB 2.0 OTG

- Support High-Speed (HS, 480Mbps), Full-Speed (FS, 12Mbps), and Low-Speed (LS, 1.5Mbps) in Host mode
- Support High-Speed (HS, 480Mbps) and Full-Speed (FS, 12Mbps) in Device mode
- Support up to five configurable endpoints for bulk, isochronous, control and interrupt

USB Host

- EHCI/OHCI-compliant host
- USB2.0 PHY and HSIC

LRADC

- 6-bit resolution

Digital Audio Interface

- Two I2S/PCM compliant digital audio interfaces for modem and bluetooth
- I2S supports 2 channels output and 2 channels input
- PCM supports linear sample(8-bit or 16-bit), 8-bit u-law and A-law companded sample

UART

- Support six UART controllers
- Support FIFO size up to 64 bytes
- Support speed up to 3MHz

SPI

- Support two SPI controllers with one chip select signal
- Master/Slave configurable

TWI

- Support four TWI controllers
- Support one dedicated TWI controller for CSI
- Support speed up to 400Kbps

RSB™ (Reduced Serial Bus)

- Support transfer speed up to 20MHz

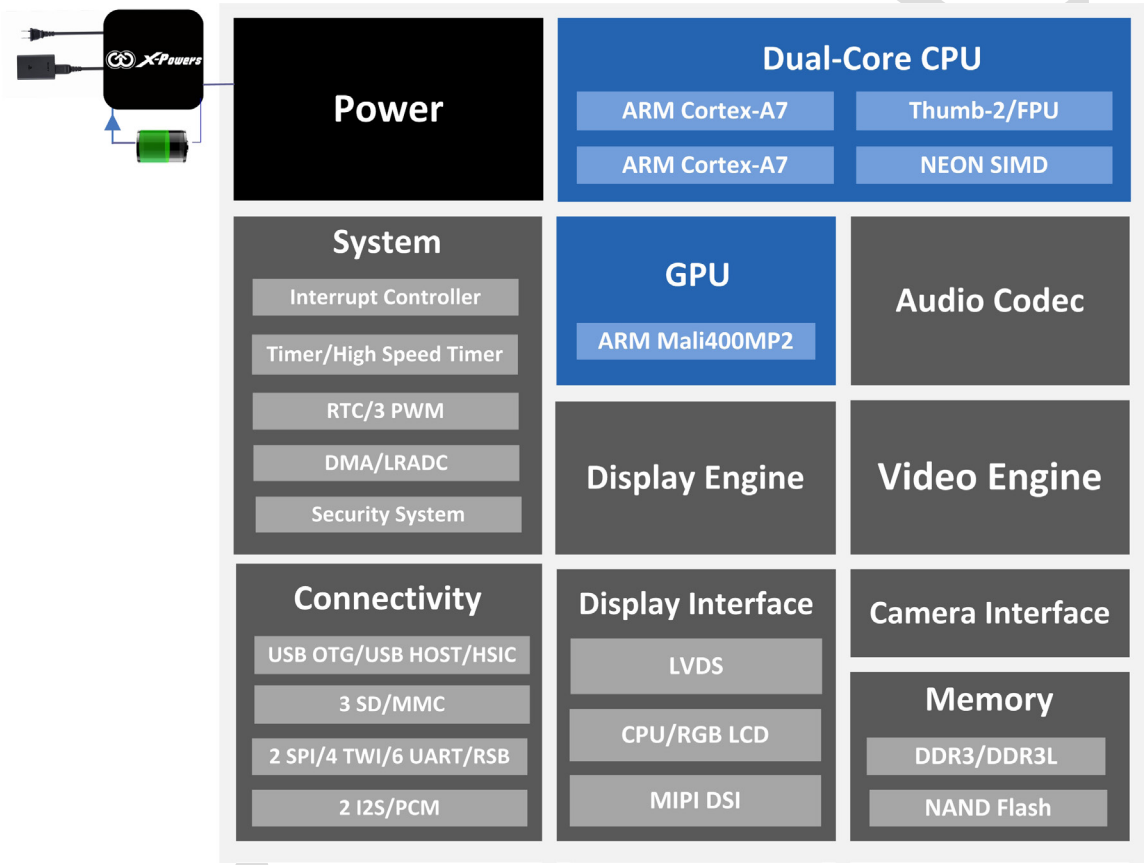
2.10. Power Management

- Support DVFS for CPU frequency and voltage adjustment
- Support super standby mode for energy efficiency
- Support talking standby mode for energy efficiency during voice call application

2.11. Process and Package

- 40nm LP process
- FBGA 280 balls,0.80mm ball pitch, 14 x 14 x 1.4-mm

3 BLOCK DIAGRAM



A23 Block Diagram

4 PIN DESCRIPTION

4.1. PIN CHARACTERISTICS

Following table describes the A2x pin characteristics from seven aspects: ***BALL#, Pin Name, Default Function[1], Type[2], Reset State[3], Default Pull Up/Down[4], and Buffer Strength[5]***.

BALL#	Pin Name	Default Function	Type	Reset State	Default Pull Up/Down	Buffer Strength (mA)
SDRAM						
M1	DQ0	DRAM	I/O	Z	-	-
M2	DQ1	DRAM	I/O	Z	-	-
L1	DQ2	DRAM	I/O	Z	-	-
L2	DQ3	DRAM	I/O	Z	-	-
J1	DQ4	DRAM	I/O	Z	-	-
J2	DQ5	DRAM	I/O	Z	-	-
H1	DQ6	DRAM	I/O	Z	-	-
H2	DQ7	DRAM	I/O	Z	-	-
U3	DQ8	DRAM	I/O	Z	-	-
U1	DQ9	DRAM	I/O	Z	-	-
U2	DQ10	DRAM	I/O	Z	-	-
T2	DQ11	DRAM	I/O	Z	-	-
R2	DQ12	DRAM	I/O	Z	-	-
P1	DQ13	DRAM	I/O	Z	-	-
P2	DQ14	DRAM	I/O	Z	-	-
N1	DQ15	DRAM	I/O	Z	-	-
M4	DVREF	DRAM	P	-	-	-
R1	DQS1	DRAM	I/O	Z	-	-
T1	DQS1B	DRAM	I/O	Z	-	-
T3	DQM1	DRAM	O	Z	-	-
K2	DQS0	DRAM	I/O	Z	-	-
K1	DQS0B	DRAM	I/O	Z	-	-
N2	DQM0	DRAM	O	Z	-	-

Note:

1 ***Default function*** defines the default function of each pin, especially for pins with multiplexing functions;

2 There are five ***pin types*** here: O for output, I for input, I/O for input/output, A for analog,OD for Open-Drain, P for power and G for ground;

3 ***Reset state*** defines the state of the terminal at reset: Z for high-impedance.

4 ***Default Pull up/down*** defines the presence of an internal pull up or pull down resistor. Unless otherwise specified, the pin is default to be floating, and can be configured as pull up or pull down;

5 ***Buffer strength*** defines the driver strength of the associated output buffer. It is tested in the condition that VCC= 3.0V, strength=MAX;

BALL#	Pin Name	Default Function	Type	Reset State	Default Pull Up/Down	Buffer Strength (mA)
G2	DCKB	DRAM	O	Z	-	-
G1	DCK	DRAM	O	Z	-	-
J4	DCKE	DRAM	O	Z	-	-
E4	DA0	DRAM	O	Z	-	-
D1	DA1	DRAM	O	Z	-	-
F2	DA2	DRAM	O	Z	-	-
H3	DA3	DRAM	O	Z	-	-
D2	DA4	DRAM	O	Z	-	-
F1	DA5	DRAM	O	Z	-	-
A1	DA6	DRAM	O	Z	-	-
G4	DA7	DRAM	O	Z	-	-
B1	DA8	DRAM	O	Z	-	-
F4	DA9	DRAM	O	Z	-	-
E2	DA10	DRAM	O	Z	-	-
C2	DA11	DRAM	O	Z	-	-
E1	DA12	DRAM	O	Z	-	-
F3	DA13	DRAM	O	Z	-	-
C1	DA14	DRAM	O	Z	-	-
E3	DA15	DRAM	O	Z	-	-
J3	DBA0	DRAM	O	Z	-	-
K4	DBA1	DRAM	O	Z	-	-
H4	DBA2	DRAM	O	Z	-	-
K3	DWE	DRAM	O	Z	-	-
M3	DCAS	DRAM	O	Z	-	-
L4	DRAS	DRAM	O	Z	-	-
N3	DCS	DRAM	O	Z	-	-
L3	DODT	DRAM	O	Z	-	-
R3	DZQ	DRAM	A	Z	-	-
G3	DRST	DRAM	O	Z	-	-
P3	VDD-DLL	POWER	P	-	-	-
H5,J5,K5,L5, H6,J6	VCC-DRAM	POWER	P	-	-	-
N4	GND-DLL	GROUND	G	-	-	-
GPIO B						
G17	PB0	GPIO	I/O	Z	NO PULL	20
G16	PB1	GPIO	I/O	Z	NO PULL	20
F17	PB2	GPIO	I/O	Z	NO PULL	20
F16	PB3	GPIO	I/O	Z	NO PULL	20
G14	PB4	GPIO	I/O	Z	NO PULL	20
G15	PB5	GPIO	I/O	Z	NO PULL	20
F14	PB6	GPIO	I/O	Z	NO PULL	20
F15	PB7	GPIO	I/O	Z	NO PULL	20
GPIO C						
D12	PC0	GPIO	I/O	Z	NO PULL	20
C12	PC1	GPIO	I/O	Z	NO PULL	20
C11	PC2	GPIO	I/O	Z	NO PULL	20
D11	PC3	GPIO	I/O	Z	PULL UP	20
B11	PC4	GPIO	I/O	Z	PULL UP	20
C10	PC5	GPIO	I/O	Z	NO PULL	20
D10	PC6	GPIO	I/O	Z	PULL UP	20

BALL#	Pin Name	Default Function	Type	Reset State	Default Pull Up/Down	Buffer Strength (mA)
A12	PC7	GPIO	I/O	Z	NO PULL	20
A11	PC8	GPIO	I/O	Z	NO PULL	20
B10	PC9	GPIO	I/O	Z	NO PULL	20
A10	PC10	GPIO	I/O	Z	NO PULL	20
B9	PC11	GPIO	I/O	Z	NO PULL	20
A9	PC12	GPIO	I/O	Z	NO PULL	20
B8	PC13	GPIO	I/O	Z	NO PULL	20
A8	PC14	GPIO	I/O	Z	NO PULL	20
B7	PC15	GPIO	I/O	Z	NO PULL	20
A7	PC16	GPIO	I/O	Z	NO PULL	20
GPIO D						
R12	PD2	GPIO	I/O	Z	NO PULL	20
P12	PD3	GPIO	I/O	Z	NO PULL	20
R11	PD4	GPIO	I/O	Z	NO PULL	20
P11	PD5	GPIO	I/O	Z	NO PULL	20
R10	PD6	GPIO	I/O	Z	NO PULL	20
P10	PD7	GPIO	I/O	Z	NO PULL	20
R9	PD10	GPIO	I/O	Z	NO PULL	20
P9	PD11	GPIO	I/O	Z	NO PULL	20
R8	PD12	GPIO	I/O	Z	NO PULL	20
P8	PD13	GPIO	I/O	Z	NO PULL	20
R7	PD14	GPIO	I/O	Z	NO PULL	20
P7	PD15	GPIO	I/O	Z	NO PULL	20
U11	PD18	GPIO	I/O	Z	NO PULL	20
T11	PD19	GPIO	I/O	Z	NO PULL	20
U10	PD20	GPIO	I/O	Z	NO PULL	20
T10	PD21	GPIO	I/O	Z	NO PULL	20
U9	PD22	GPIO	I/O	Z	NO PULL	20
T9	PD23	GPIO	I/O	Z	NO PULL	20
U8	PD24	GPIO	I/O	Z	NO PULL	20
T8	PD25	GPIO	I/O	Z	NO PULL	20
U7	PD26	GPIO	I/O	Z	NO PULL	20
T7	PD27	GPIO	I/O	Z	NO PULL	20
M11,N11	VCC-PD	POWER	P	-	-	-
GPIO E						
C5	PE0	GPIO	I/O	Z	NO PULL	20
D5	PE1	GPIO	I/O	Z	NO PULL	20
C6	PE2	GPIO	I/O	Z	NO PULL	20
D6	PE3	GPIO	I/O	Z	NO PULL	20
A6	PE4	GPIO	I/O	Z	NO PULL	20
B6	PE5	GPIO	I/O	Z	NO PULL	20
A5	PE6	GPIO	I/O	Z	NO PULL	20
B5	PE7	GPIO	I/O	Z	NO PULL	20
A4	PE8	GPIO	I/O	Z	NO PULL	20
B4	PE9	GPIO	I/O	Z	NO PULL	20
A3	PE10	GPIO	I/O	Z	NO PULL	20
B3	PE11	GPIO	I/O	Z	NO PULL	20
A2	PE12	GPIO	I/O	Z	NO PULL	20
B2	PE13	GPIO	I/O	Z	NO PULL	20
C3	PE14	GPIO	I/O	Z	NO PULL	20

BALL#	Pin Name	Default Function	Type	Reset State	Default Pull Up/Down	Buffer Strength (mA)
D3	PE15	GPIO	I/O	Z	NO PULL	20
C4	PE16	GPIO	I/O	Z	NO PULL	20
D4	PE17	GPIO	I/O	Z	NO PULL	20
GPIO F						
D9	PF0	GPIO	I/O	Z	NO PULL	20
C9	PF1	GPIO	I/O	Z	NO PULL	20
D8	PF2	GPIO	I/O	Z	NO PULL	20
C8	PF3	GPIO	I/O	Z	NO PULL	20
D7	PF4	GPIO	I/O	Z	NO PULL	20
C7	PF5	GPIO	I/O	Z	NO PULL	20
GPIO G						
A15	PG0	GPIO	I/O	Z	NO PULL	20
B15	PG1	GPIO	I/O	Z	NO PULL	20
A14	PG2	GPIO	I/O	Z	NO PULL	20
B14	PG3	GPIO	I/O	Z	NO PULL	20
A13	PG4	GPIO	I/O	Z	NO PULL	20
B13	PG5	GPIO	I/O	Z	NO PULL	20
A17	PG6	GPIO	I/O	Z	NO PULL	20
B17	PG7	GPIO	I/O	Z	NO PULL	20
A16	PG8	GPIO	I/O	Z	NO PULL	20
B16	PG9	GPIO	I/O	Z	NO PULL	20
C17	PG10	GPIO	I/O	Z	NO PULL	20
C16	PG11	GPIO	I/O	Z	NO PULL	20
C15	PG12	GPIO	I/O	Z	NO PULL	20
C14	PG13	GPIO	I/O	Z	NO PULL	20
GPIO H						
D17	PH0	GPIO	I/O	Z	NO PULL	20
D16	PH1	GPIO	I/O	Z	NO PULL	20
D15	PH2	GPIO	I/O	Z	NO PULL	20
D14	PH3	GPIO	I/O	Z	NO PULL	20
D13	PH4	GPIO	I/O	Z	NO PULL	20
C13	PH5	GPIO	I/O	Z	NO PULL	20
E17	PH6	GPIO	I/O	Z	NO PULL	20
E16	PH7	GPIO	I/O	Z	NO PULL	20
E15	PH8	GPIO	I/O	Z	NO PULL	20
E14	PH9	GPIO	I/O	Z	NO PULL	20
GPIO L						
P16	PL0	GPIO	I/O	Z	PULL UP	20
P15	PL1	GPIO	I/O	Z	PULL UP	20
U14	PL2	GPIO	I/O	Z	NO PULL	20
T14	PL3	GPIO	I/O	Z	NO PULL	20
R14	PL4	GPIO	I/O	Z	NO PULL	20
P14	PL5	GPIO	I/O	Z	NO PULL	20
U13	PL6	GPIO	I/O	Z	NO PULL	20
T13	PL7	GPIO	I/O	Z	NO PULL	20
R13	PL8	GPIO	I/O	Z	NO PULL	20
P13	PL9	GPIO	I/O	Z	NO PULL	20
U12	PL10	GPIO	I/O	Z	NO PULL	20
T12	PL11	GPIO	I/O	Z	NO PULL	20
SYSTEM CONTROL						
N14	NMI	-	I	Z	NO PULL	-

BALL#	Pin Name	Default Function	Type	Reset State	Default Pull Up/Down	Buffer Strength (mA)
P17	RESET	-	I	Z	NO PULL	-
USB						
T16	USB-DM0	-	A	-	-	-
T17	USB-DP0	-	A	-	-	-
U16	USB-DM1	-	A	-	-	-
U17	USB-DP1	-	A	-	-	-
L12	VCC-USB	-	P	-	-	-
HSIC						
N12	VCC-HSIC		P	-	-	-
T15	HSIC-STR		A	-	-	-
U15	HSIC-DAT		A	-	-	-
AUDIO CODEC						
M16	MIC1N	-	A	-	-	-
M17	MIC1P	-	A	-	-	-
N16	MIC2N	-	A	-	-	-
N17	MIC2P	-	A	-	-	-
J15	LINEINR	-	A	-	-	-
H15	LINEINL	-	A	-	-	-
K16	VRA1	-	A	-	-	-
K17	VRA2	-	A	-	-	-
L16	AVCC	-	P	-	-	-
L17	VRP	-	A	-	-	-
N15	PHONEOUTN	-	A	-	-	-
M15	PHONEOUTP	-	A	-	-	-
K15	PHONEINN	-	A	-	-	-
L15	PHONEINP	-	A	-	-	-
G14	HBIAS	-	A	-	-	-
K14	MBIAS	-	A	-	-	-
H13	AGND	-	G	-	-	-
J16	HPOUTR	-	A	-	-	-
J17	HPOUTL	-	A	-	-	-
H14	HPCOM	-	A	-	-	-
H16	HPCOMFB	-	A	-	-	-
H17	HPVCCBP	-	P	-	-	-
K13	HPVCCIN	-	P	-	-	-
LRADC						
L14	LRADC0	-	A	-	-	-
DSI						
R4	DSI-D0N	-	A	-	-	-
P4	DSI-D0P	-	A	-	-	-
R5	DSI-D1N	-	A	-	-	-
P5	DSI-D1P	-	A	-	-	-
U6	DSI-D2N	-	A	-	-	-
T6	DSI-D2P	-	A	-	-	-
P6	DSI-D3N	-	A	-	-	-
R6	DSI-D3P	-	A	-	-	-
U5	DSI-CKN	-	A	-	-	-
T5	DSI-CKP	-	A	-	-	-
N6	VCC-DSI	-	A	-	-	-
CLOCK						
R17	X32KIN	-	A	-	-	-

BALL#	Pin Name	Default Function	Type	Reset State	Default Pull Up/Down	Buffer Strength (mA)
R16	X32KOUT	-	A	-	-	-
R15	X32KFOUT	-	A	-	-	-
M13	RTCVIO	-	A	-	-	-
M12	VCC-RTC	-	P	-	-	-
U4	X24MIN	-	A	-	-	-
T4	X24MOUT	-	A	-	-	-
M5	VCC-PLL	-	P	-	-	-
POWER						
M14	VDD-CPUS	-	P	-	-	-
E5,E6,E7,F5,F6, F7,G5,G6	VDD-CPU	-	P	-	-	-
E8,E9,E10,K6, L6,M6,M7,N8 N9,N10	VDD-SYS	-	P	-	-	-
E11,E12,F11 F12,G12	VCC-IO	-	P	-	-	-
F8,F9,F10, G7,G8,G9,G10, G11,H7,H8, H9,H10,H11, H12,J7,J8,J9, J10,J11,J12 K7,K8,K9,K10, K11,K12,L7, L8,L9,L10, L11, M8,M9,M10	GND	-	G	-	-	-

4.2. GPIO MULTIPLEXING FUNCTIONS

Following table provides a description of the GPIO multiplexing functions of A23.

Port	Default Function	IO Type	Default IO State	Default Pull Up/Down	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3
PB0	GPIO	I/O	DIS	Z	UART2_TX	-	PB_EINT0
PB1	GPIO	I/O	DIS	Z	UART2_RX	-	PB_EINT1
PB2	GPIO	I/O	DIS	Z	UART2_RTS	-	PB_EINT2
PB3	GPIO	I/O	DIS	Z	UART2_CTS	-	PB_EINT3
PB4	GPIO	I/O	DIS	Z	PCM0_SYNC	-	PB_EINT4
PB5	GPIO	I/O	DIS	Z	PCM0_CLK	-	PB_EINT5
PB6	GPIO	I/O	DIS	Z	PCM0_DOUT	-	PB_EINT6
PB7	GPIO	I/O	DIS	Z	PCM0_DIN	-	PB_EINT7
PC0	GPIO	I/O	DIS	Z	NAND_WE	SPI0_MOSI	-
PC1	GPIO	I/O	DIS	Z	NAND_ALE	SPI0_MISO	-
PC2	GPIO	I/O	DIS	Z	NAND_CLE	SPI0_CLK	-
PC3	GPIO	I/O	DIS	Pull-up	NAND_CE1	SPI0_CS	-
PC4	GPIO	I/O	DIS	Pull-up	NAND_CE0	-	-
PC5	GPIO	I/O	DIS	Z	NAND_RE	SDC2_CLK	-
PC6	GPIO	I/O	DIS	Pull-up	NAND_RB0	SDC2_CMD	-
PC7	GPIO	I/O	DIS	Pull-up	NAND_RB1	-	-
PC8	GPIO	I/O	DIS	Z	NAND_DQ0	SDC2_D0	-
PC9	GPIO	I/O	DIS	Z	NAND_DQ1	SDC2_D1	-
PC10	GPIO	I/O	DIS	Z	NAND_DQ2	SDC2_D2	-
PC11	GPIO	I/O	DIS	Z	NAND_DQ3	SDC2_D3	-
PC12	GPIO	I/O	DIS	Z	NAND_DQ4	SDC2_D4	-
PC13	GPIO	I/O	DIS	Z	NAND_DQ5	SDC2_D5	-
PC14	GPIO	I/O	DIS	Z	NAND_DQ6	SDC2_D6	-
PC15	GPIO	I/O	DIS	Z	NAND_DQ7	SDC2_D7	-
PC16	GPIO	I/O	DIS	Z	NAND_DQS	SDC2_RST	-
PD2	GPIO	I/O	DIS	Z	LCD_D2	SDC1_CLK	-
PD3	GPIO	I/O	DIS	Z	LCD_D3	SDC1_CMD	-
PD4	GPIO	I/O	DIS	Z	LCD_D4	SDC1_D0	-
PD5	GPIO	I/O	DIS	Z	LCD_D5	SDC1_D1	-
PD6	GPIO	I/O	DIS	Z	LCD_D6	SDC1_D2	-
PD7	GPIO	I/O	DIS	Z	LCD_D7	SDC1_D3	-
PD10	GPIO	I/O	DIS	Z	LCD_D10	UART1_TX	-
PD11	GPIO	I/O	DIS	Z	LCD_D11	UART1_RX	-
PD12	GPIO	I/O	DIS	Z	LCD_D12	UART1_RTS	-
PD13	GPIO	I/O	DIS	Z	LCD_D13	UART1_CTS	-
PD14	GPIO	I/O	DIS	Z	LCD_D14		-
PD15	GPIO	I/O	DIS	Z	LCD_D15		-
PD18	GPIO	I/O	DIS	Z	LCD_D18	LVDS_VP0	-
PD19	GPIO	I/O	DIS	Z	LCD_D19	LVDS_VN0	-
PD20	GPIO	I/O	DIS	Z	LCD_D20	LVDS_VP1	-
PD21	GPIO	I/O	DIS	Z	LCD_D21	LVDS_VN1	-
PD22	GPIO	I/O	DIS	Z	LCD_D22	LVDS_VP2	-
PD23	GPIO	I/O	DIS	Z	LCD_D23	LVDS_VN2	-
PD24	GPIO	I/O	DIS	Z	LCD_CLK	LVDS_VPC	-
PD25	GPIO	I/O	DIS	Z	LCD_DE	LVDS_VNC	-

PD26	GPIO	I/O	DIS	Z	LCD_HSYNC	LVDS_VP3	-
PD27	GPIO	I/O	DIS	Z	LCD_VSYNC	LVDS_VN3	-
PE0	GPIO	I/O	DIS	Z	CSI_PCLK	-	-
PE1	GPIO	I/O	DIS	Z	CSI_MCLK	-	-
PE2	GPIO	I/O	DIS	Z	CSI_HSYNC	-	-
PE3	GPIO	I/O	DIS	Z	CSI_VSYNC	-	-
PE4	GPIO	I/O	DIS	Z	CSI_D0	-	-
PE5	GPIO	I/O	DIS	Z	CSI_D1	-	-
PE6	GPIO	I/O	DIS	Z	CSI_D2	-	-
PE7	GPIO	I/O	DIS	Z	CSI_D3	-	-
PE8	GPIO	I/O	DIS	Z	CSI_D4	-	-
PE9	GPIO	I/O	DIS	Z	CSI_D5	-	-
PE10	GPIO	I/O	DIS	Z	CSI_D6	-	-
PE11	GPIO	I/O	DIS	Z	CSI_D7	-	-
PE12	GPIO	I/O	DIS	Z	CSI_SCK	TWI2_SCK	-
PE13	GPIO	I/O	DIS	Z	CSI_SDA	TWI2_SDA	-
PE14	GPIO	I/O	DIS	Z	-	-	-
PE15	GPIO	I/O	DIS	Z	-	-	-
PE16	GPIO	I/O	DIS	Z	-	-	-
PE17	GPIO	I/O	DIS	Z	-	-	-
PF0	GPIO	I/O	JTAG	Z	SDC0_D1	-	-
PF1	GPIO	I/O	JTAG	Z	SDC0_D0	-	-
PF2	GPIO	I/O	DIS	Z	SDC0_CLK	-	-
PF3	GPIO	I/O	JTAG	Z	SDC0_CMD	-	-
PF4	GPIO	I/O	DIS	Z	SDC0_D3	-	-
PF5	GPIO	I/O	JTAG	Z	SDC0_D2	-	-
PG0	GPIO	I/O	DIS	Z	SDC1_CLK	-	PG_EINT0
PG1	GPIO	I/O	DIS	Z	SDC1_CMD	-	PG_EINT1
PG2	GPIO	I/O	DIS	Z	SDC1_D0	-	PG_EINT2
PG3	GPIO	I/O	DIS	Z	SDC1_D1	-	PG_EINT3
PG4	GPIO	I/O	DIS	Z	SDC1_D2	-	PG_EINT4
PG5	GPIO	I/O	DIS	Z	SDC1_D3	-	PG_EINT5
PG6	GPIO	I/O	DIS	Z	UART1_TX	-	PG_EINT6
PG7	GPIO	I/O	DIS	Z	UART1_RX	-	PG_EINT7
PG8	GPIO	I/O	DIS	Z	URAT1_RTS	-	PG_EINT8
PG9	GPIO	I/O	DIS	Z	UART1_CTS	-	PG_EINT9
PG10	GPIO	I/O	DIS	Z	PCM1_SYNC	-	PG_EINT10
PG11	GPIO	I/O	DIS	Z	PCM1_CLK	-	PG_EINT11
PG12	GPIO	I/O	DIS	Z	PCM1_DOUT	-	PG_EINT12
PG13	GPIO	I/O	DIS	Z	PCM1_DIN	-	PG_EINT13
PH0	GPIO	I/O	DIS	Z	PWM0	-	-
PH1	GPIO	I/O	DIS	Z	PWM1	-	-
PH2	GPIO	I/O	DIS	Z	TWI0_SCK	-	-
PH3	GPIO	I/O	DIS	Z	TWI0_SDA	-	-
PH4	GPIO	I/O	DIS	Z	TWI1_SCK	-	-
PH5	GPIO	I/O	DIS	Z	TWI1_SDA	-	-
PH6	GPIO	I/O	DIS	Z	SPI0_CS	UART3_TX	-
PH7	GPIO	I/O	DIS	Z	SPI0_CLK	UART3_RX	-
PH8	GPIO	I/O	DIS	Z	SPI0_DOUT	UART_RTS	-
PH9	GPIO	I/O	DIS	Z	SPI0_DIN	UART_CTS	-
PL0	GPIO	I/O	DIS	Pull-up	S_RSB_SCK	S_TWI_SCK	S_PL_EINT0
PL1	GPIO	I/O	DIS	Pull-up	S_RSB_SDA	S_TWI_SDA	S_PL_EINT1
PL2	GPIO	I/O	DIS	Z	S_UART_TX	-	S_PL_EINT2
PL3	GPIO	I/O	DIS	Z	S_UART_RX	-	S_PL_EINT3
PL4	GPIO	I/O	DIS	Z		-	S_PL_EINT4

PL5	GPIO	I/O	DIS	Z		-	S_PL_EINT5
PL6	GPIO	I/O	DIS	Z		-	S_PL_EINT6
PL7	GPIO	I/O	DIS	Z		-	S_PL_EINT7
PL8	GPIO	I/O	DIS	Z	S_TWI_SCK	-	S_PL_EINT8
PL9	GPIO	I/O	DIS	Z	S_TWI_SDA	-	S_PL_EINT9
PL10	GPIO	I/O	DIS	Z	S_PWM	-	S_PL_EINT10
PL11	GPIO	I/O	DIS	Z	-	-	S_PL_EINT11

4.3. DETAILED PIN/SIGNAL DESCRIPTION

Pin/Signal	Description	Type
DRAM		
DQ[15:0]	DRAM DQ[15:0]	I/O
DVREF	DRAM Reference Input	P
DQS[1:0]	DRAM Data Strobe DQS[1:0]	I/O
DQSB[1:0]	DRAM Data Strobe DQSB[1:0]	I/O
DCK	DRAM Clock	O
DCKB	DRAM CKB	O
DCKE	DRAM Clock Enable	O
DA[15:0]	DRAM Data Address[15:0]	O
DBA[2:0]	DRAM Bank Address[2:0]	O
DWE	DRAM Write Enable	O
DCAS	DRAM Column Address Strobe	O
DRAS	DRAM Row Address Strobe	O
DCS	DRAM Chip Select	O
DODT	DRAM ODT Control	O
DZQ	DRAM ZQ Calibration	A
DRST	DRAM Reset	O
VDD-DLL	DLL Power Supply	P
VCC-DRAM	DRAM Power Supply	P
GPIO		
PB[7:0]	Port B Bit[7:0]	I/O
PC[18:0]	Port C Bit[18:0]	I/O
PD[27:0]	Port D Bit[27:0]	I/O
VCC-PD	Port D Power Supply	P
PE[17:0]	Port E Bit[17:0]	I/O
PF[5:0]	Port F Bit[5:0]	I/O
PG[13:0]	Port G Bit[13:0]	I/O
PH[9:0]	Port H Bit[9:0]	I/O
PL[11:0]	Port L Bit[11:0]	I/O
SYSTEM CONTROL		
NMI	Non-Maskable Interrupt	I
RESET	Reset Signal	I
INTERRUPT		
EINT	External Interrupt	I
PWM		
PWM[1:0]	PWM	O
CLOCK		
X32KIN	Clock Input of 32768Hz Crystal	A

Pin/Signal	Description	Type
X32KOUT	Clock Output of 32768Hz Crystal	A
X32KFOUT	Clock Output of LOSC (X32KFOUT can be gating)	OD
RTCVIO	RTC Power	P
VCC-RTC	RTC Power Supply	P
X24MIN	Clock Input of 24MHz Crystal	A
X24MOUT	Clock Output of 24MHz Crystal	A
VCC-PLL	PLL Power	P
NAND FLASH		
NAND-DQ[7:0]	NAND Flash Data Bit[7:0]	I/O
NAND-CE[1:0]	NAND Flash Chip Select[1:0]	O
NAND-WE	NAND Flash Write Enable	O
NAND-ALE	NAND Flash Address Latch Enable	O
NAND-CLE	NAND Flash Command Latch Enable	O
NAND-RE	NAND Flash Read Enable	O
NAND-RB	NAND Flash Ready/Busy Bit	I
NAND-DQS	NAND Flash Data Strobe	I/O
LCD		
LCD-D[23:0]	LCD Data Bit[23:0]	O
LCD-CLK	LCD Clock Signal	O
LCD-DE	LCD Data Enable	O
LCD-HSYNC	LCD Horizontal SYNC	O
LCD-VSYNC	LCD Vertical SYNC	O
LVDS		
LVDS-VP[3:0]	LVDS Data Positive Signal Output[3:0]	A
LVDS-VN[3:0]	LVDS Data Negative Signal Output[3:0]	A
LVDS-VPC	LVDS Clock Positive Output	A
LVDS-VNC	LVDS Clock Negative Output	A
DSI		
DSI-DN(3:0)	DSI Data Negative	A
DSI-DP(3:0)	DSI Data Positive	A
DSI-CKN	DSI Clock Negative	A
DSI-CKP	DSI Clock Positive	A
VCC-DSI	DSI Power Supply	P
CSI		
CSI-D[7:0]	CSI0 Data Bit[7:0]	I
CSI-PCLK	CSI Pixel Clock	I
CSI-MCLK	CSI Master Clock	O
CSI-SCK	CSI Clock Signal	O
CSI-SDA	CSI Data Signal	IO
CSI-HSYNC	CSI Horizontal SYNC	I
CSI-VSYNC	CSI Vertical SYNC	I
USB		
USB-DM[1:0]	USB DM[1:0] Signal	A
USB-DP[1:0]	USB DP[1:0] Signal	A
VCC-USB	USB Power Supply	P
HSIC		
VCC-HSIC	HSIC Power Supply	P
HSIC-STR	USB HSIC signal	A
HSIC-DAT	USB HSIC signal	A
AUDIO CODEC		
PHONEOUTN	Phone Negative Output	A
PHONEOUTP	Phone Positive Output	A
PHONEINN	Phone Negative Input	A

Pin/Signal	Description	Type
PHONEINP	Phone Positive Input	A
MICINN[2:1]	MIC Negative Input	A
MICINP[2:1]	MIC Positive Input	A
LINEINR	Line-in Right Input	A
LINEINL	Line-in Left Input	A
HBIAS	HBIAS	A
MBIAS	MBIAS	A
VRA1	Reference (1.5V)	A
VRA2	Reference (1.5V)	A
AVCC	Analog Power Supply	P
VRP	Reference (3.0V)	A
AGND	Analog Ground	G
HPOUTR	Headphone Right Channel Output	A
HPOUTL	Headphone Left Channel Output	A
HPVCCIN	Headphone VCC Input	A
HPVCCBP	Headphone VCC Bypass	A
HPCOM	Headphone Common Reference	A
HPCOMFB	Headphone Common Reference Feedback	A
HPBP	Headphone Bypass Output	A
LRADC		
LRADC0	LRADC Input	A
SPI		
SPI0-CS	SPI Chip Select Signal	I/O
SPI0-CLK	SPI Clock Signal	I/O
SPI0-DOUT	SPI Data Output	O
SPI0-DIN	SPI Data Input	I
SPI0-MOSI	SPI Master Data Out, Slave Data In	I/O
SPI0-MISO	SPI Master Data In, Slave Data Out	I/O
UART (x=[3:0])		
UARTx-TX	UART Data Transmit	O
UARTx-RX	UART Data Receive	I
UARTx-RTS	UART Data Request to Send	O
UARTx-CTS	UART Data Clear to Send	I
TWI (x=[2:0])(Open-Drain)		
TWIx-SCK	TWI Clock Signal	I/O
TWIx-SDA	TWI Data Signal	I/O
SD/MMC (x=[2:0])		
SDCx-D	SD/MMC/SDIO Data Bit	I/O
SDCx-CLK	SD/MMC/SDIO Clock	O
SDCx-CMD	SD/MMC/SDIO Command Signal	I/O
SDC-RST	SD/MMC/SDIO Reset Signal	O
PCM(x=[1:0])		
PCMx-SYNC	PCM SYNC	I/O
PCMx-CLK	PCM Clock	I/O
PCMx-DOUT	PCM Data Output	O
PCMx-DIN	PCM Data Input	I
RSB		
S-RSB-SCK	RSB Clock	O
S-RSB-SDA	RSB Data	I/O
POWER		
VDD-CPU	CPU Power Supply	P
VDD-CPUS	CPUS Power Supply	P
VDD-SYS	System Power Supply	P

Pin/Signal	Description	Type
GND	Ground	G
VCC-IO	IO Power Supply	P

5 ELECTRICAL CHARACTERISTICS

5.1. ABSOLUTE MAXIMUM RATINGS

Functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

SYMBOL	PARAMETER		MIN	MAX	UNIT
T_g	Storage Temperature		-65	150	°C
$I_{I/O}$	In/Out current for input and output		-	-	mA
V_{ESD}	ESD stress voltage	HBM(human body model)	-4000	+4000	V_{ESD}
		CDM(charged device model)	NA	NA	
VCC-IO	DC Supply Voltage for I/O		-	3.6	V
VDD-DLL	Power Supply for DLL		-	2.75	V
VCC-DRAM	Power Supply for DRAM (DDR3L)		-	1.35	V
	Power Supply for DRAM (DDR3)		-	1.5	V
VCC-PLL	Power Supply for PLL		-	3.3	V
VCC-RTC	Power Supply for RTC		-	3.3	V
AVCC	DC Supply Voltage for Analog Part		-	3.3	V
VCC-USB	Power Supply for USB PHY		-	3.6	V
VCC-DSI	Power Supply for DSI		-	3.6	V
VDD-CPU	Power Supply for CPU		-	1.3	V
VDD-SYS	Power Supply for System		-	1.3	V

5.2. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_a	Ambient Operating Temperature[Commercial]	-20	-	70	°C
	Operating Temperature[Extended]	NA	NA	NA	°C
GND	Ground	0	0	0	V
VCC-IO	DC Supply Voltage for I/O	1.8	3.0	3.6	V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
VDD-DLL	Power Supply for DLL	2.37	2.5	2.63	V
VCC-DRAM	Power Supply for DRAM (DDR3L)	-	1.35	-	V
	Power Supply for DRAM (DDR3)	-	1.5	-	V
VCC-PLL	Power Supply for PLL	2.85	3.0	3.15	V
VCC-USB	Power Supply for USB PHY	2.7	3.3	3.6	V
VCC-RTC	Power Supply for RTC	2.85	3.0	3.15	V
AVCC	DC Supply Voltage for Analog Part	2.8	3.0	3.3	V
VCC-DSI	Power Supply for MIPI DSI	3.14	3.3	3.47	V
VDD-CPU	Power Supply for CPU	1.0	-	1.3	V
VDD-SYS	Power Supply for System	1.0	-	1.3	V

5.3. DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-Level Input Voltage	VCC-IO=3.0V	2.1	3.0	3.6	V
V_{IL}	Low-Level Input Voltage	VCC-IO=3.0V	-0.3	0	0.7	V
V_{HYS}	Hysteresis Voltage	-	-	-	-	mV
I_{IH}	High-Level Input Current	VCC-IO=3.0V, VI=3.0V	TBD	TBD	TBD	uA
I_{IL}	Low-Level Input Current	VCC-IO=3.0V, VI=0V	TBD	TBD	TBD	uA
V_{OH}	High-Level Output Voltage	VCC-IO=3.0V	2.7	3.0	NA	V
V_{OL}	Low-Level Output Voltage	VCC-IO=3.0V	NA	0	0.4	V
I_{OZ}	Tri-State Output Leakage Current	VCC-IO=3.0V	TBD	TBD	TBD	uA
C_{IN}	Input Capacitance	-	NA	NA	5	pF
C_{OUT}	Output Capacitance	-	NA	NA	5	pF

5.4. OSCILLATOR ELECTRICAL CHARACTERISTICS

The A23 contains two oscillators: a 24MHz oscillator and a 32768Hz oscillator. Each oscillator requires a specific crystal.

The A23 device operation requires following two input clocks:

- The 32768Hz frequency is used for low frequency operation.
- The 24MHz frequency is used to generate the main source clock of the A23 device.

5.4.1. 24MHz OSCILLATOR CHARACTERISTICS

The 24MHz crystal is connected between the HOSCI (amplifier input) and HOSCO (amplifier output).

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
1/(tCPMAIN)	Crystal Oscillator Frequency Range	-	24	-	MHz
t_{ST}	Startup Time	-	-	-	ms
	Frequency Tolerance at 25°C	-50	-	50	ppm
	Oscillation Mode	Fundamental			-
	Maximum Change Over Temperature Range	-50	-	50	ppm
PON	Drive Level	-	-	50	uW
CL	Equivalent Load Capacitance	-	-	-	pF
CL1,CL2	Internal Load Capacitance(CL1=CL2)	-	-	-	pF
RS	Series Resistance(ESR)	-	-	-	Ω
	Duty Cycle	30	50	70	%
CM	Motional Capacitance	-	-	-	pF
C_{SHUT}	Shunt Capacitance	-	-	-	pF
R_{BIAS}	Internal Bias Resistor	-	-	-	MΩ

5.4.2. 32768HZ OSCILLATOR CHARACTERISTICS

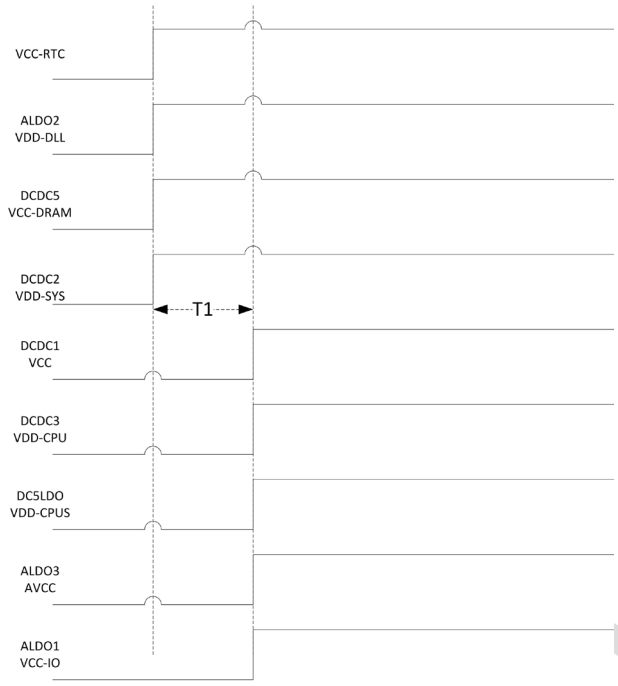
The 32768Hz crystal is connected between the LOSCI (amplifier input) and LOSCO (amplifier output).

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
1/(tCPMAIN)	Crystal Oscillator Frequency Range	-	32768	-	Hz
t_{ST}	Startup Time	-	-	-	ms
	Frequency Tolerance at 25°C	-50	-	50	ppm
	Oscillation Mode	Fundamental			-
	Maximum Change Over Temperature Range	-50	-	50	ppm
PON	Drive Level	-	-	50	uW
CL	Equivalent Load Capacitance	-	-	-	pF
CL1,CL2	Internal Load Capacitance(CL1=CL2)	-	-	-	pF
RS	Series Resistance(ESR)	-	-	-	Ω
	Duty Cycle	30	50	70	%
CM	Motional Capacitance	-	-	-	pF
C_{SHUT}	Shunt Capacitance	-	-	-	pF
R_{BIAS}	Internal Bias Resistor	-	-	-	MΩ

5.5. POWER UP/DOWN SEQUENCE

The external voltage regulator and other power-on devices must provide the processor with a specific sequence of power and resets to ensure proper operations.

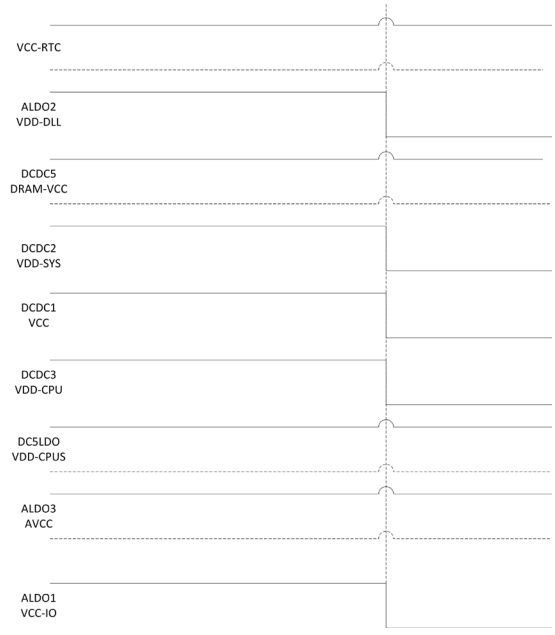
Power On Sequence



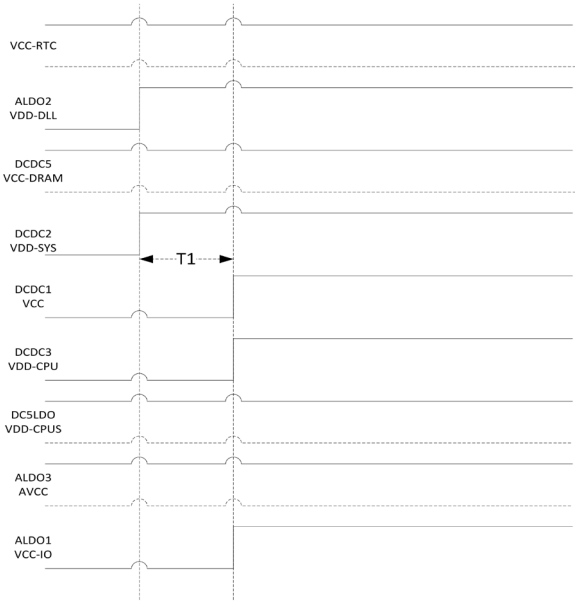
Note: 1ms < T1 < 100ms； Typically, T1=4ms

Power Off Sequence

Enter Super Standby/ Talking Standby



Exit Super Standby/Talking Standby



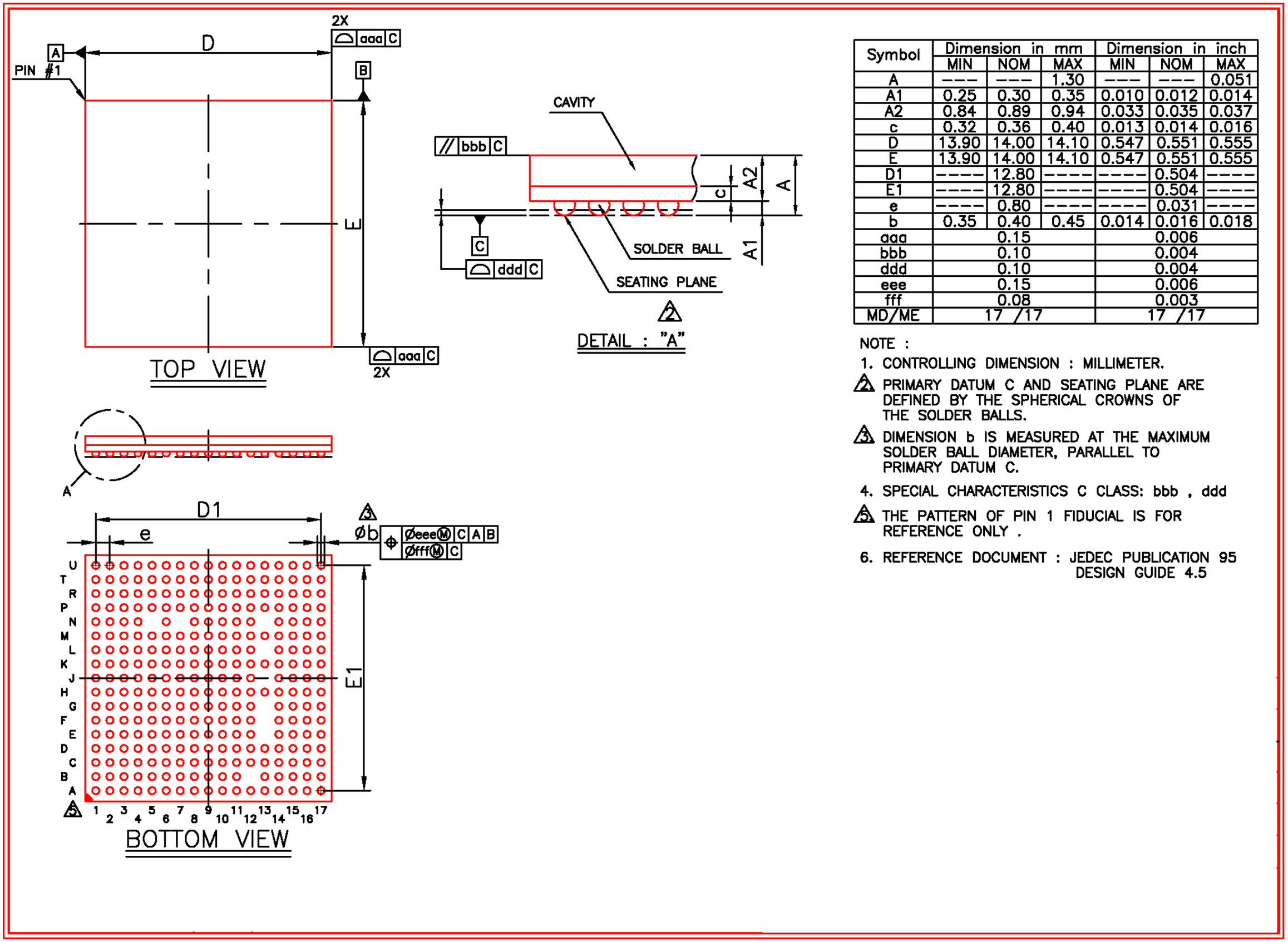
Note:1ms < T1 < 100ms; Typically, T1=4ms

6 PIN ASSIGNMENT

6.1. PIN MAP

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	DA6	PE12	PE10	PE8	PE6	PE4	PC16	PC14	PC12	PC10	PC8	PC7	PG4	PG2	PG0	PG9	PG6	A
B	DA8	PE13	PE11	PE9	PE7	PE5	PC15	PC13	PC11	PC9	PC4		PG5	PG3	PG1	PG8	PG7	B
C	DA14	DA11	PE14	PE16	PE0	PE2	PF5	PF3	PF1	PC5	PC2	PC1	PH5	PG13	PG12	PG11	PG10	C
D	DA1	DA4	PE15	PE17	PE1	PE3	PF4	PF2	PF0	PC6	PC3	PC0	PH4	PH3	PH2	PH1	PH0	D
E	DA12	DA10	DA15	DA0	VDD-CPU	VDD-CPU	VDD-CPU	VDD-SYS	VDD-SYS	VDD-SYS	VCC-IO	VCC-IO		PH9	PH8	PH7	PH6	E
F	DA5	DA2	DA13	DA9	VDD-CPU	VDD-CPU	VDD-CPU	GND	GND	GND	VCC-IO	VCC-IO		PB6	PB7	PB3	PB2	F
G	DCK	DCKB	DRST	DA7	VDD-CPU	VDD-CPU	GND	GND	GND	GND	GND	VCC-IO		PB4	PB5	PB1	PB0	G
H	DQ6	DQ7	DA3	DBA2	VCC-DRAM	VCC-DRAM	GND	GND	GND	GND	GND	GND	AGND	HPCOM	LINEINL	HPCOMFB	HPVCCBP	H
J	DQ4	DQ5	DBA0	DCKE	VCC-DRAM	VCC-DRAM	GND	GND	GND	GND	GND	GND		HBIAS	LINEINR	HPOUTR	HPOUTL	J
K	DQS0B	DQS0	DWE	DBA1	VCC-DRAM	VDD-SYS	GND	GND	GND	GND	GND	GND	HPVCCIN	MBIAS	PHONEINN	VRA1	VRA2	K
L	DQ2	DQ3	DODT	DRAS	VCC-DRAM	VDD-SYS	GND	GND	GND	GND	GND	VCC-USB		LRADC0	PHONEINP	AVCC	VRP	L
M	DQ0	DQ1	DCAS	DVREF	VCC-PLL	VDD-SYS	VDD-SYS	GND	GND	GND	VCC-PD	VCC-RTC	RTCVIO	VDD-CPUS	PHONEOUTP	MIC1N	MIC1P	M
N	DQ15	DQM0	DCS	GND-DLL		VCC-DSI		VDD-SYS	VDD-SYS	VDD-SYS	VCC-PD	VCC-HSIC		NMI	PHONEOUTN	MIC2N	MIC2P	N
P	DQ13	DQ14	VDD-DLL	DSI-D0P	DSI-D1P	DSI-D3P	PD15	PD13	PD11	PD7	PD5	PD3	PL9	PL5	PL1	PL0	RESET	P
R	DQS1	DQ12	DZQ	DSI-D0N	DSI-D1N	DSI-D3N	PD14	PD12	PD10	PD6	PD4	PD2	PL8	PL4	X32KFOUT	X32KOUT	X32KIN	R
T	DQS1B	DQ11	DQM1	X24MOUT	DSI-CKP	DSI-D2P	PD27	PD25	PD23	PD21	PD19	PL11	PL7	PL3	HSIC-STR	USB-DM0	USB-DP0	T
U	DQ9	DQ10	DQ8	X24MIN	DSI-CKN	DSI-D2N	PD26	PD24	PD22	PD20	PD18	PL10	PL6	PL2	HSIC-DAT	USB-DM1	USB-DP1	U
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

6.2. PACKAGE DIMENSION



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.30	---	---	0.051
A1	0.25	0.30	0.35	0.010	0.012	0.014
A2	0.84	0.89	0.94	0.033	0.035	0.037
c	0.32	0.36	0.40	0.013	0.014	0.016
D	13.90	14.00	14.10	0.547	0.551	0.555
E	13.90	14.00	14.10	0.547	0.551	0.555
D1	----	12.80	----	----	0.504	----
E1	----	12.80	----	----	0.504	----
e	----	0.80	----	----	0.031	----
b	0.35	0.40	0.45	0.014	0.016	0.018
aaa		0.15			0.006	
bbb		0.10			0.004	
ddd		0.10			0.004	
eee		0.15			0.006	
fff		0.08			0.003	
MD/ME		17 /17			17 /17	

NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. SPECIAL CHARACTERISTICS C CLASS: bbb , ddd
5. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY .
6. REFERENCE DOCUMENT : JEDEC PUBLICATION 95 DESIGN GUIDE 4.5

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