Allwinner Technology

A31

Datasheet

Version 1.4

2013/12/10

REVISION HISTORY

Version	Date	Author	Description
1.0	Nov 6, 2012		Initial version
1.1	Feb 27, 2013		Modify the A31 block diagram
1.2	March 21, 2013		Revise video output spec
1.21	June 30, 2013		Revise the logo
1.3	Sep 20, 2013		Modify the electrical characteristic section
1.4	Dec,10,2013		Modify Pin Description

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1 OVERVIEW

A31 is a highly integrated mobile application processor designed to provide high performance solutions for tablets, handsets, and smart TVs, etc.

It comes with a Quad-core Cortex-A7 CPU architecture that allows outstanding computing capability with less power consumption, a powerful SGX544 GPU with eight logic cores, and a robust multimedia processing system that capable of 4Kx2K video decoding, Blu-ray 3D and perfect compatibility for stream media, etc.

A31 also features dual-channel 32bitx2 DRAM bus to provide wider bandwidth, and dual-channel NAND flash to speed up Read/Write operations.

Besides, A31 provides a board range of peripheral interfaces. For example, it comes with display interfaces such as HDMI, LCD RGB, MIPI DSI, and LVDS, image input interfaces such as CSI and MIPI CSI, and data interfaces such as USB DRD, USB EHCI/OHCI, GB Ethernet, SDC, SDIO, etc.

When it comes to power efficiency, A31 features smart Power Consumption Management System to dynamically adjust CPU frequency and voltage, DRAM Dynamic Frequency Scaling technology to dynamically adjust DRAM frequency based on bandwidth requirements, and also supports Super Standby Mode to lower the power consumption during system standby.

2 FEATURE

CPU Architecture

- Quad Cortex-A7 Subsystem
  - ARM Version 7 ISA standard ARM instruction set plus Thumb-2, Jazeller RCT
  - 32KB instruction and 32KB data L1 cache for each CPU
  - NEON SIMD coprocessor and VFPV4 for each CPU
  - TrustZone security technology
  - Hardware virtualization support
  - Large Physical Address Extensions(LPAE)
  - Debug and trace features
  - One general timer for each CPU
  - Shared 1MB L2 cache
- CPUS
  - Support 4KB I-cache
  - Support 64KB SRAM (instruction space)
  - Support 64KB secure SRAM (data space)

GRAPHIC ENGINE

- **3D**
  - Power VR SGX544 MP2 GPU
  - Support Open GL ES 2.0 /Open VG 1.1 / Open CL 1.1 / DX 9.3 standard

- **2D**
  - Support BLT / ROP2/3/4, scaling function with 4x4 taps and 32 phases
  - Support 90/180/270 rotation degree, mirror/alpha (plane and pixel alpha)/ color key
  - Any format conversion：ARGB 8888/4444/1555, RGB565, Mono 1/2/4/8 bpp, Palette 1/2/4/8 bpp (input only), YUV 444/422/420
  - Support command queue

MEMORY SUBSYSTEM

- **Internal Boot ROM**
  - 32KB
  - Support system boot from 8-bit NAND Flash, SPI Nor Flash (SPI0) and SD /TF /8-bit eMMC (SDC0/2)
  - Support system code download via USB DRD (USB0)
- **External SDRAM**
  - Comply to LPDDR1/2, DDR2, DDR3 SDRAM jedec specification
  - Dual Channels SDRAM Controller
  - Support memory device power of 1.2V/1.35V/1.5V/1.8V
  - Memory capacity up to 16G bits
  - Up to two chip select signals for each channel
  - 16 address lines and 3 bank address lines per channel
  - Support LPDDR1/2, DDR2, DDR3 SDRAM
  - Support 8/16/32 bits bus width per DRAM chip

- **NAND FLASH**
  - Comply to ONFI 2.3 & toggle 1.0
  - Up to 2 channels
  - Support 64 bits ECC per 512 bytes or 1024 bytes
  - Support 8bits/16bits data bus width
  - Support 1K/2K/4K/8K/16K page size
  - Support up to 4 CE and 2 RB
  - Support hardware randomize engine
  - Support system boot from NAND flash
  - Support SLC/MLC/TLC NAND and EF-NAND
  - Support SDR/DDR NAND interface
  - Support internal DMA controller for data transfer

- **SD/MMC**
  - Comply to eMMC standard specification v4.5
  - Comply to SD physical layer specification v3.0
  - Comply to SDIO card specification v2.0
  - 1/4/8 bits bus width
  - Support HS/DS/SDR12/SDR25/SDR50 /HS200/ DDR50 bus mode
  - Support eMMC mandatory and alternative boot operations
  - Transmit clock up to100MHz
  - Support four independent SD/MMC/SDIO controllers
  - Support SDSC/SDHC/SDXC/UHS-I/MMC/ RS-MMC card

- Support eMMC/iNand Flash
- Support 1GB/2GB/4GB/8GB/16GB/32GB/64GB /128GB SD/MMC card
- Support SDIO interrupt detection
- Support descriptor-based internal DMA controller for efficient scatter and gather operations

SYSTEM RESOURCES

- **Timer**
  - 6 timers: clock source can be switched over 24M/32K for all timers, and external signals can function as clock source for timer4/5
  - 33-bit AVS counter
  - 4 watchdogs to generate reset signal or interrupts
- **GIC**
  - Support 16 SGIs, 16 PPIs, and 128 SPIs
  - Support ARM architecture security extensions
  - Support ARM architecture virtualization extensions
  - Uni-processor and multiprocessor environments
- **HS-Timer**
  - 4 channels
  - Clock source fixed to AHB, and pre-scale ranges from 1 to 16
  - 56-bit counter, can be separated to 24-bit Hi-register and 32-bit Low-register
- **DMA**
  - 16 channels
  - Support data width of 8/16/32 bits
  - Support linear and IO address modes
  - DMA channels can be paused during data transfer if necessary
- **RTC**
  - Real time registers for second, minute, hour, day, month and year
  - Two alarms based on seconds and weeks
  - 16 general purpose registers
- **CCU**
  - 11 programmable PLLs

IMAGE SIGNAL PROCESSOR

- Support image mirror flip and rotation
- Support thumb image generation
- Support two channels output
- Support valid picture size up to 4096x4096
- Support speed up to 250M pixel/s
- ISP for YCbCr input
  - YCbCr gain and offset control
  - DRC(dynamic range compression)
  - Anti-flick detection statistics
  - Histogram statistics
- ISP for RAW RGB input
  - Black clamp with horizontal/vertical offset compensation
  - Window capture
  - Static/dynamic defect pixel correction
  - Super lens shading correction
  - Super lens flare correction
  - Color dependent gain and offset control
  - Anisotropic non-linear bayer interpolation with false color suppression
  - Programmable color correction
  - Programmable gamma correction
  - DRC(dynamic range compression)
  - RGB2YCbCr
  - Non-linear 2D sharpening
  - Advanced contrast enhancement
  - Advanced spatial (2D) de-noise filter
  - Zone-based AE/AF/AWB statistics
  - Anti-flick detection statistics
  - Histogram statistics

VIDEO ENGINE

- Decoder and encoder can work at the same time
- Video decoding
  - Picture size up to 4096x2304
  - Decoding speed up to 1920x1080@60fps
  - Support multiple video formats: Mpeg1, Mpeg2, Mpeg4 SP/ASP GMC, H.263 including Sorenson Spark, H.264 BP/MP/HP, VP6/8, AVS jizun, JPEG/MJPEG
  - Support tiled/YUV/YUV output format
- Video Encoding
  - H.264 HP: picture size up to 3840x2160
  - H.264 HP: speed up to 1920x1080@60fps
  - H.264 HP: cyclic intra refresh
  - H.264 HP: ROI windows
  - JPEG baseline: picture size up to 8192x8192
  - Alpha blending
  - Thumb generation
  - 4x2 scaling ratio: from 1/16 to 64 arbitrary non-integer ratio

DISPLAY ENGINE

- Support dual display paths
  - Each path supports 4 movable and size-adjustable layers
  - Layer size up to 8192x8192 pixels
- Ultra-scaling Engine
  - 8 taps in horizontal and 4 taps in vertical
  - Source image size from 8x4 to 8192x8192
  - Destination image size from 8x4 to 8192x8192
- Support multiple image input formats
  - Mono 1/2/4/8 bpp

- Palette 1/2/4/8 bpp
- 16/24/32 bpp color
- YUV444/420/422/411

- Support alpha blending, color key, gamma, hardware cursor
- Support powerful video post processing
  - De-interlacing
  - Detail enhancement
  - Dynamic range control
  - Color management
- 3D content input/output format conversion and display (with HDMI)

VIDEO OUTPUT

- Support HDMI 1.4, speed up to 3G bps per channel, resolution up to 1080p@60fps
- Dual flexible sync RGB/CPU/LVDS LCD interface, up to 1080p@60fps
- Support 4 lanes MIPI DSI, 1G bps per lane, resolution up to 1920x1200/1080p@60fps
- Support dual display devices processing

VIDEO INPUT

- Support 4 lanes MIPI CSI, 1G bps per lane (up to 12M pixels still image or 1080p@60fps video)
- Support parallel 12-bit CSI

ANALOG AUDIO OUTPUT

- Two-channel audio DAC
- Stereo capless headphone drivers
  - Up to 100dBA SNR for DAC playback
  - 8KHz~192KHz DAC sample rate
- Support analog/digital volume control
- Two low-noise analog microphone bias
- Dedicated headphone/speaker/earpiece outputs, single-ended or differential
- Support differential phone-out
- Support two mixers for different applications
  - Output mixer for LINEINL/R, PHONEP/N, MIC1P/N, MIC2P/N and stereo DAC output
  - ADC record mixer for LINEINL/R, PHONEP/N, MIC1P/N, MIC2P/N, MIC3P/N, stereo DAC output
- Flexible digital audio process for DAC
  - Pop suppression control
  - Individual high pass filter/De-emphasis filter
  - Support EQ equalization
  - Soft volume control and soft mute

ANALOG AUDIO INPUT

- Support two audio ADC channels
  - 96dBA SNR for ADC recording
  - 8KHz~ 48KHz ADC sample rate
- Analog low-power loop from line-in/mic-in/ phone-in to headphone/speaker/ earpiece outputs
- Accessory button press detection
- Five analog audio inputs
  - Three differential microphone inputs
  - Differential phone-in input
  - Stereo line-in input
- Support low-noise digital MIC interface
- Flexible digital audio process for ADC
  - High pass filter and low latency decimation filter for class voice
  - Automatic gain control (AGC)

GPADC

- Support 12-bit resolution
- Conversion rate up to 1MSPS
- Low power consumption
- 3V power supply
- Analog input range: 0V~3V
- On-chip sample-and-hold function
- Single or multiple input channel select mode
- Median and averaging filter to reduce noise

CONNECTIVITY

- **USB2.0 DRD**
  - Support High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps), and Low-Speed (LS, 1.5-Mbps) in Host mode
  - Support High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps) in Device mode
  - Support up to 10 user-configurable endpoints for bulk , isochronous**,** control and interrupt bi-directional transfers

- **USB EHCI/OHCI**
  - Two EHCI/OHCI-compliant Hosts
  - One OHCI only FS Host

- **LRADC**
  - Support 6-bit resolution
  - Support 0V ~2V voltage input

- **Digital Audio Interface**
  - Comply to industry standard I2S/PCM specification
  - Two sets I2S/PCM interfaces for baseband and Bluetooth
  - Support Master/Slave mode and full-duplex operation
  - Support 8KHz ~192KHz audio sample rate
  - Support MCLK output for CODEC chips
  - Support standard I2S, left-justified, right-justified, 8/16-bit linear sample, 8-bit u-law and a-law companded sample

- **PWM**
  - 4 PWM outputs

- Support cycle mode and pulse mode
- The pre-scale ranges from 1 to 64

■ **Transport Stream**
- Support both SPI and SSI
- Support 64 channels PID filter
- Support hardware PCR packet detection
- Speed up to 150Mbps for both SPI and SSI interface

■ **EMAC**
- Comply to IEEE 802.3-2002 standard
- Options for automatic Pad/CRC stripping on receive frames
- Programmable frame length to support standard or Jumbo Ethernet frames with size up to 16KB
- Support 10/100/1000-Mbps transfer rates
- IEEE 802.3-compliant GMII/MII interface to communicate with an external Gigabit/Fast Ethernet PHY
- Support 10/100/1000-Mbps data transfer rates RGMII interface to communicate with an external Giga bit PHY

■ **CIR**
- A flexible receiver for IR remote controller

■ **UART**
- Comply to industry-standard 16450/16550 UARTS specification
- Support fully AMBA APB CPU interface programmable operation
- Support 16-bit programmable baud rate and dynamic modification
- Support 2-wire serial communication
- Support 4-wire auto data flow communication
- Support 8-wire modem(data carrier equipment, DCE) or data set
- Support up to 6 UART controllers

■ **One Wire Interface**
- Support both standard One Wire protocol and simple HDQ protocol

■ **SPI**
- Master/Slave configurable
- Up to 4 independent SPI controllers, SPI0 with only one CS signal for system boot, and SPI1/2/3 with two CS signals
- Support dual-input and dual-output operation

■ **TWI**
- Up to 5 TWIs compliant with I2C protocol
- Support SCCB protocol

■ **P2WI (Push-Pull TWI)**
- Support speed up to 2MHz

SECURITY SYSTEM

■ Support AES, DES, 3DES, SHA-1, MD5
■ Support ECB, CBC modes for AES/DES/3DES
■ 128-bit, 192-bit and 256-bit key size for AES
■ 160-bit hardware PRNG with 192-bit seed
■ Security JTAG

DRM SYSTEM

■ The security access permission of each address region are programmable
■ Data transfer between master and slave is permitted only when AXI transaction access permission status matches the access permission settings of the memory region it addresses
■ The write access of various registers can be prevented after the assertion of secure_boot_lock
■ Support SMTA (secure memory touch arbiter) to program some memory areas as secure or non-secure
■ Support 64KB secure SRAM size
■ Support DRAMC with firewall to configure the security attribute of different masters, such as DMA
■ Can only be accessed by CPUS

POWER MANAGEMENT

■ Flexible PLL clock generator and 32768Hz OSC
■ Flexible clock gate and module reset
■ Support DVFS for CPU frequency and voltage adjustment
■ Support dynamic frequency adjustment for external DRAM controller
■ Support standby mode

PROCESS & PACKAGE

■ FBGA 609 balls, 0.65mm ball pitch, 18 x 18 x 1.4-mm

3 BLOCK DIAGRAM

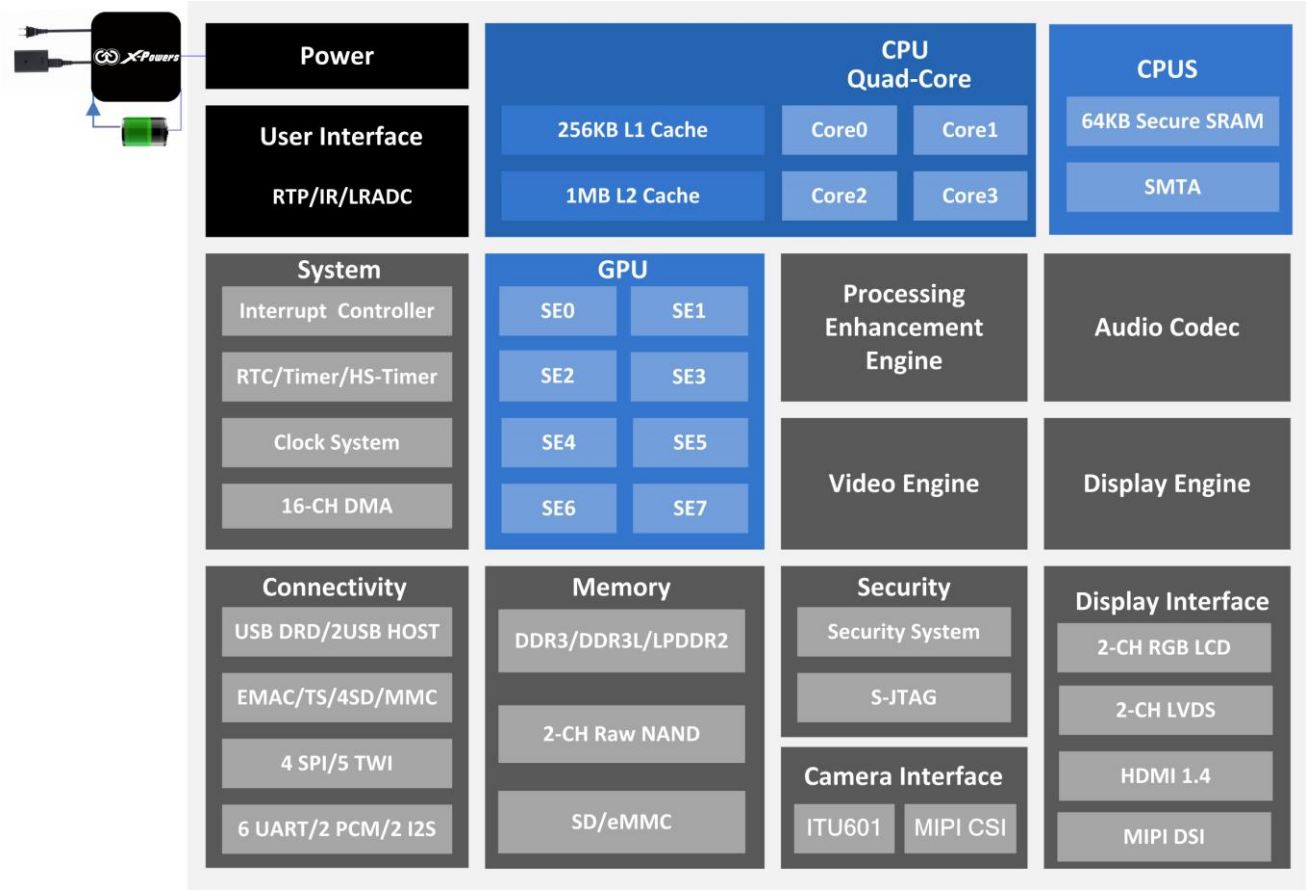


Figure 3-1. A31 Block Diagram

4 PIN ASSIGNMENT

4.1. BALL MAP

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	PC10	PC11	PC12	PC13	PC17	PC21	PC26	PH3	PH7	PH15	PH19	UBOOT	PE7
B	PC6	PC7	PC8	PC9	PC16	PC20	PC25	PH2	PH6	PH14	PH18	PH30	PE3
C	PF4	PF5	PC2	PC5	PC4	PC19	PC23	PH1	PH5	PH17	PH13	PE0	PE5
D	PF3	PC0	PC15	PC1	PC3	PC18	PC22	PH0	PH4	PH8	PH16	PH20	PE1
E	PF2	PF0	PF1	PC14									
F	S0DQ8	S0DQ14	S0DQ2	S0DQ6		PC27	PC24	PH10	PH9	PH24	PH26	PH28	PH22
G	S0DQ12	S0DQ10	S0DQ0	S0DQ4		VCC-PF	VCC-PC	VCC-PC	PH11	PH12	PH23	PH21	PH25
H	S0DQS1B	S0DQS1	S0DQS0	S0DQS0B		S0ZQ	VCC-DRAM						
J	S0DQ15	S0DQ13	S0DQ1	S0DQ7		S0ODT1	VCC-DRAM		VDD-GPU	VDD-GPU	VDD-GPU	GND	GND
K	S0DQ9	S0DQ11	S0DQ5	S0DQ3		S0CS1	VCC-DRAM		VDD-GPU	VDD-GPU	VDD-GPU	GND	GND
L	S0ODT	S0DQM1	S0DQM0	S0RAS		S0CKE1	VCC-DRAM		VDD-GPU	VDD-GPU	VDD-GPU	GND	GND
M	S0WE	S0BA0	S0CS	S0CAS		VCC-DRAM	VCC-DRAM		VDD-GPU	VDD-GPU	VDD-GPU	GND	GND
N	S0A5	S0A0	S0BA2	S0A3		VCC-DRAM	VCC-DRAM		GND	GND	GND	GND	GND

Figure 4-1 A31 Ball Map (Upper Left)）

14	15	16	17	18	19	20	21	22	23	24	25	26	27	
PE8	PE12	PE14	PG3	PG7	PG9	PG15	PG18	PB2	PA1	PA2	PA6	PA10	PA14	A
PE4	PE11	PE15	PG2	PG6	PG10	PG16	PB0	PB3	PB6	PA3	PA7	PA11	PA15	B
PE6	PE10	PE16	PG1	PG4	PG12	PG14	PB1	PB4	PA0	PA5	PA9	PA12	PA16	C
PE2	PE9	PE13	PG0	PG5	PG11	PG13	PG17	PB5	PB7	PA4	PA8	PA13	PA17	D
										PA18	PA19	PA20	PA21	E
PH29	TEST	BOOTSEL0	JTAGSEL0	VCC-PE	PG8	VCC-PA	CPU-VDDFB	GND		PA25	PA22	PA23	PA24	F
PH27	VCC-PH	BOOTSEL1	JTAGSEL1	VCC-PG	VCC-PB	VCC-PA	VCC-HP	TPX1		HPCOM	HPCOMFB	PA26	PA27	G
							CPU-VDDSW	VRP		HPOUTL	HPOUTR	LINEINL	LINEINR	H
VCC-PH	VDD-CPU	VDD-CPU	VDD-CPU	VDD-CPU	AGND		TPY2	VRA2		PHINP	PHINN	MIC1N	MIC1P	J
GND	VDD-CPU	VDD-CPU	VDD-CPU	VDD-CPU	VDD-CPU		PM2	VRA1		MIC2P	MIC2N	MBIAS	HBIAS	K
GND	VDD-CPU	VDD-CPU	VDD-CPU	VDD-CPU	VDD-CPU		TPY1	AVCC		LINEOUTR	LINEOUTL	PHOUTP	PHOUTN	L
GND	VDD-CPU	VDD-CPU	VDD-CPU	VDD-CPU	VDD-CPU		MIC3P	PM3		LRADC1	LRADC0	PM0	PM1	M
GND	VDD-CPU	VDD-CPU	VDD-CPU	VDD-CPU	HPBP		MIC3N	TPX2		PM4	PM5	PM6	PM7	N

Figure 4-2 A31 Ball Map (Upper Right)）

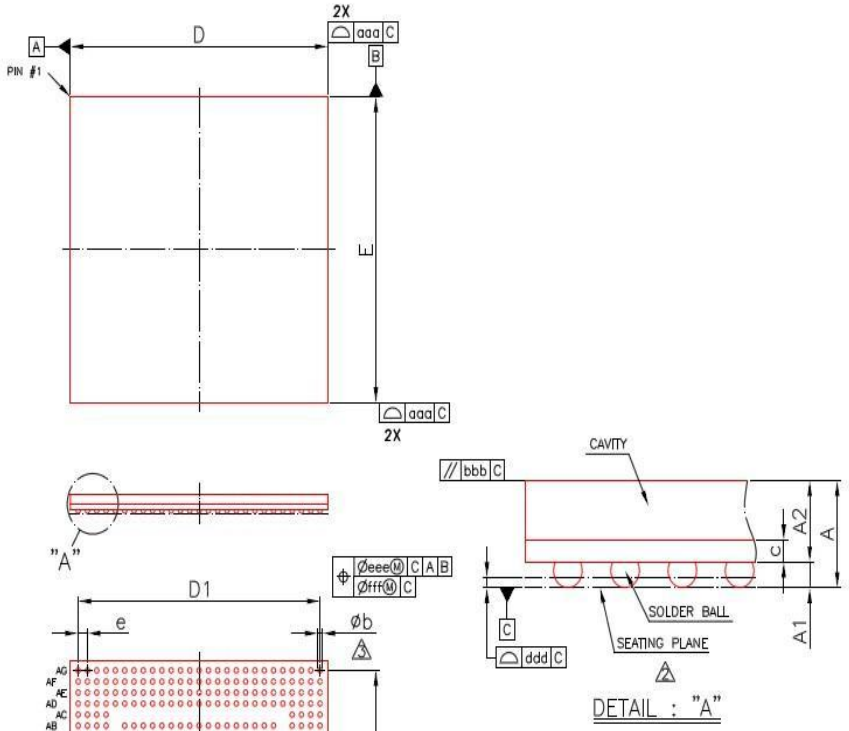
	1	2	3	4	5	6	7	8	9	10	11	12	13
P	S0CK	S0A2	S0A7	S0A9		VCC-DRAM	VCC-DRAM		GND	GND	GND	GND	GND
R	S0CKB	S0CKE	S0A13	S0RST		S0VREF	VCC-DRAM		GND	GND	GND	GND	GND
T	S0BA1	S0A10	S0A12	S0A15		S0ADBG	VCC-DRAM		GND-DRAM	GND-DRAM	GND	GND	VDD-SYS
U	S0A6	S0A11	S0A4	S0A1		S0DDBG0	VCC-DRAM		GND-DRAM	GND-DRAM	GND	GND	VDD-SYS
V	S0DQ30	S0DQ26	S0A8	S0A14		S0DDBG1	GND-DRAM		VDD-DLL	GND-DRAM	GND	GND	VDD-SYS
W	S0DQ24	S0DQ28	S0DQ20	S0DQ18		GND-DRAM	GND-DRAM		VDD-DLL	GND-DRAM	GND	GND	VDD-SYS
Y	S0DQS3	S0DQS3B	S0DQ22	S0DQ16		GND-DRAM	GND-DRAM						
AA	S0DQ29	S0DQ31	S0DQS2B	S0DQS2		GND-DRAM	GND-DRAM	VCC-DRAM	VCC-DRAM	VCC-DRAM	VCC-DRAM	VCC-DRAM	VCC-DRAM
AB	S0DQ27	S0DQ25	S0DQ21	S0DQ23		S1VREF	S1ZQ	S1ODT1	S1CS1	S1CKE1	S1ADBG	S1DDBG0	S1DDBG1
AC	S0DQM3	S0DQM2	S0DQ19	S0DQ17									
AD	S1DQ6	S1DQ4	S1DQS0B	S1DQ5	S1DQ3	S1RAS	S1CAS	S1BA2	S1A2	S1RST	S1A10	S1A1	S1A14
AE	S1DQ2	S1DQ0	S1DQS0	S1DQ7	S1DQ1	S1DQM0	S1CS	S1BA0	S1A7	S1A13	S1A11	S1A6	S1A4
AF	S1DQ14	S1DQ10	S1DQS1	S1DQ11	S1DQ13	S1ODT	S1WE	S1A0	S1A9	S1CKE	S1A15	S1A8	S1DQ28
AG	S1DQ12	S1DQ8	S1DQS1B	S1DQ15	S1DQ9	S1DQM1	S1A3	S1A5	S1CK	S1CKB	S1A12	S1BA1	S1DQ30

Figure 4-3 A31 Ball Map (Lower Left)

GND	GND	GND	GND	GND	VDDQE		VDD-CPUS	VDD-CPUS		NMI	RESET	X32KI	PL0	P
GND	GND	GND	GND	GND	VCC-PM		VCC-RTC	PL3		PL2	PL1	PL4	X32KO	R
VDD-SYS	VDD-SYS	GND	GND	GND	VIO-RTC		PL5	PL8		PD0	PD1	USB-DM0	USB-DP0	T
VDD-SYS	VDD-SYS	GND	GND	GND	GND		PL6	PL7		PD2	PD3	USB-DM1	USB-DP1	U
VDD-SYS	VDD-SYS	GND	PLL-TEST	GND-PLL	VCC-PLL		VCC-PD	VCC-USB		PD4	PD5	USB-DM2	USB-DP2	V
VDD-SYS	VDD-SYS	VCC-MIPI	PLL-VREG	PLL-DV	VCC-HDMI		VCC-PD	VCC-PD		PD6	PD7	PD10	PD11	W
							GND	GND		PD8	PD9	PD12	PD13	Y
VCC-DRAM	GND-DRAM	GND-DRAM	GND-DRAM	GND	GND	GND	GND	GND		PD21	PD20	PD14	PD15	AA
GND-DRAM	GND-DRAM	GND-DRAM	GND-DRAM	GND	GND	GND	HSCL	HHPD		PD23	PD22	PD16	PD17	AB
										PD24	HSDA	PD18	PD19	AC
S1DQ18	S1DQ16	S1DQS2	S1DQ17	S1DQ21	DSI-D0N	DSI_D1N	DSI-CKN	DSI-D2N	DSI-D3N	GND	PD27	PD26	PD25	AD
S1DQ22	S1DQ20	S1DQS2B	S1DQ23	S1DQ19	DSI-D0P	DSI-D1P	DSI-CKP	DSI-D2P	DSI-D3P	GND	GND	HTX2N	HTX2P	AE
S1DQ24	S1DQS3B	S1DQ31	S1DQ25	S1DQM2	CSI2-D0N	CSI2_D1N	CSI2-CKN	CSI2-D2N	CSI2-D3N	X24MO	HTXCP	HTX0P	HTX1P	AF
S1DQ26	S1DQS3	S1DQ29	S1DQ27	S1DQM3	CSI2-D0P	CSI2-D1P	CSI2-CKP	CSI2-D2P	CSI2-D3P	X24MI	HTXCN	HTX0N	HTX1N	AG
14	15	16	17	18	19	20	21	22	23	24	25	26	27	

Figure 4-4 A31 Ball Map (Lower Right)）

4.2. PIN DIMENSION



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.40	---	---	0.055
A1	0.16	0.21	0.26	0.006	0.008	0.010
A2	0.84	0.89	0.94	0.033	0.035	0.037
c	0.32	0.36	0.40	0.013	0.014	0.016
D	17.90	18.00	18.10	0.705	0.709	0.713
E	17.90	18.00	18.10	0.705	0.709	0.713
D1	---	16.90	---	---	0.665	---
E1	---	16.90	---	---	0.665	---
e	---	0.65	---	---	0.026	---
b	0.25	0.30	0.35	0.010	0.012	0.014
aaa	0.15			0.006		
bbb	0.15			0.006		
ddd	0.13			0.005		
eee	0.15			0.006		
fff	0.08			0.003		
MD/ME	27/27			27/27		

NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. REFERANCE DOCUMENT : JEDEC PUBLICATION 95 DESIGN GUIDE 4.5
5. SPECIAL CHARACTERISTICS C CLASS: bbb, ddd (SPIL STANDARD.)
6. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY .

Figure 4-5. A31 Pin Dimension

5 PIN DESCRIPTION

5.1. PIN CHARACTERISTICS

Table 5-1 lists the characteristics of A31 609 Pins.

NOTES

1) **Pin Name** defines the names of pins. Note that a group of pins with similar meaning may be expressed in the form of [x:0], and their corresponding ball is given in BALL# column in increasing order, for example, for pin group S0DQ[31:0], G3 is the ball# of S0DQ0, J3 is the ball# of S0DQ1, F3 is the ball# of S0DQ2, etc;
2) **Default Function** defines the default function of each pin;
3) **Type** defines the signal direction: I (Input), O (Output), I/O(Input / Output), A (Analog), P (Power), G (Ground);
4) **Default IO State** defines the default IO state of each pin: DIS means *disable;*
5) **Default Pull Up/Down** defines the presence of an internal pull up or pull down resister. Unless otherwise specified, the pin is default to be floating, and can be configured as pull up or pull down; Note that the NMI and RESET pins require no additional pull-up resistors;
6) **Buffer Strength** defines drive strength of the associated output buffer. It is tested in the condition that VCC= 3.3V, strength=MAX;
7) P[A:M] in Table 5-1 stands for GPIO [A:M]. For detailed auxiliary functions of each GPIO, please go to Section 5.2 GPIO Multiplexing Functions section.

Ball#	Pin Name[1]	Default Function[2]	Type[3]	Default IO State[4]	Default Pull Up/Down[5]	Buffer Strength[6] (mA)	Power Supply
DRAM							
G3,J3,F3,K4,G4,K3,F4,J4,F1,K1,G2,K2,G1,J2,F2,J1,Y4,AC4,W4,AC3,W3,AB3,Y3,AB4,W1,AB2,V2,ABI,W2,AA1,V1,AA2	S0DQ[31:0]	DRAM	I/O	DIS	Z	-	
H3,H2,AA4,Y1	S0DQS[3:0]	DRAM	I/O	DIS	Z	-	
H4,H1,AA3,Y2	S0DQSB[3:0]	DRAM	I/O	DIS	Z	-	
L3,L2,AC2,AC1	S0DQM[3:0]	DRAM	O	DIS	Z	-	
P1	S0CK	DRAM	O	DIS	Z	-	
R1	S0CKB	DRAM	O	DIS	Z	-	
R2,L6	S0CKE[1:0]	DRAM	O	DIS	Z	-	VCC_DRAM
N2,U4,P2,N4,U3,N1,U1,P3,V3,P4,T2,U2,T3,R3,V4,T4	S0A[15:0]	DRAM	O	DIS	Z	-	
M1	S0WE	DRAM	O	DIS	Z	-	
M4	S0CAS	DRAM	O	DIS	Z	-	
L4	S0RAS	DRAM	O	DIS	Z	-	
M3,K6	S0CS[1:0]	DRAM	O	DIS	Z	-	
M2,T1,N3	S0BA[2:0]	DRAM	O	DIS	Z	-	
L1,J6	S0ODT[1:0]	DRAM	O	DIS	Z	-	
R4	S0RST	DRAM	O	DIS	Z	-	

Ball#	Pin Name[1]	Default Function[2]	Type[3]	Default IO State[4]	Default Pull Up/Down[5]	Buffer Strength[6] (mA)	Power Supply
H6	S0ZQ	DRAM	A	-	-	-	
R6	S0VREF	DRAM	P	-	-	-	
H7,J7,K7,L7,M6,M7,N6,N7,P6,P7,R7,T7,U7,AA8,AA9,AA10,AA11,AA12,AA13,AA14	VCC-DRAM (20)	DRAM	P	-	-	-	
T9,T10,U9,U10,V7,V10,W6,W7,W10,Y6,Y7,AA6,AA7,AA15,AA16,AA17,AB14,AB15,AB16,AB17	GND-DRAM (20)	DRAM	G	-	-	-	
V9,W9	VDD-DLL	DRAM	P	-	-	-	
T6	S0ADBG	DRAM	A	-	-	-	
U6	S0DDBG0	DRAM	A	-	-	-	
V6	S0DDBG1	DRAM	A	-	-	-	
AE2,AE5,AE1,AD5,AD2,AD4,AD1,AE4,AG2,AG5,AF2,AF4,AG1,AF5,AF1,AG4,AD15,AD17,AD14,AE18,AE15,AD18,AE14,AE17,AF14,AF17,AG14,AG17,AF13,AG16,AG13,AF16	S1DQ[31:0]	DRAM	I/O	DIS	Z	-	
AE3,AF3,AD16,AG15	S1DQS[3:0]	DRAM	I/O	DIS	Z	-	
AD3,AG3,AE16,AF15	S1DQSB[3:0]	DRAM	I/O	DIS	Z	-	
AE6,AG6,AF18,AG18	S1DQM[3:0]	DRAM	O	DIS	Z	-	
AG9	S1CK	DRAM	O	DIS	Z		
AG10	S1CKB	DRAM	O	DIS	Z	-	
AF10,AB10	S1CKE[1:0]	DRAM	O	DIS	Z	-	
AF8,AD12,AD9,AG7,AE13,AG8,AE12,AE9,AF12,AF9,AD11,AE11,AG11,AE10,AD13,AF11	S1A[15:0]	DRAM	O	DIS	Z	-	
AF7	S1WE	DRAM	O	DIS	Z	-	VCC-DRAM
AD7	S1CAS	DRAM	O	DIS	Z	-	
AD6	S1RAS	DRAM	O	DIS	Z	-	
AE7,AB9	S1CS[1:0]	DRAM	O	DIS	Z	-	
AE8,AG12,AD8	S1BA[2:0]	DRAM	O	DIS	Z	-	
AF6,AB8	S1ODT[1:0]	DRAM	O	DIS	Z	-	
AD10	S1RST	DRAM	O	DIS	Z	-	
AB7	S1ZQ	DRAM	A	-	-	-	
AB6	S1VREF	DRAM	P	-	-	-	
AB11	S1ADGB	DRAM	A	-	-	-	
AB12	S1DDBG0	DRAM	A	-	-	-	
AB13	S1DDBG1	DRAM	A	-	-	-	
GPIO A[7]							
C23	PA0	GPIO	I/O	DIS	Z	20	
A23	PA1	GPIO	I/O	DIS	Z	20	
A24	PA2	GPIO	I/O	DIS	Z	20	VCC-PA
B24	PA3	GPIO	I/O	DIS	Z	20	
D24	PA4	GPIO	I/O	DIS	Z	20	

Ball#	Pin Name[1]	Default Function[2]	Type[3]	Default IO State[4]	Default Pull Up/Down[5]	Buffer Strength[6] (mA)	Power Supply
C24	PA5	GPIO	I/O	DIS	Z	20	
A25	PA6	GPIO	I/O	DIS	Z	20	
B25	PA7	GPIO	I/O	DIS	Z	20	
D25	PA8	GPIO	I/O	DIS	Z	20	
C25	PA9	GPIO	I/O	DIS	Z	20	
A26	PA10	GPIO	I/O	DIS	Z	20	
B26	PA11	GPIO	I/O	DIS	Z	20	
C26	PA12	GPIO	I/O	DIS	Z	20	
D26	PA13	GPIO	I/O	DIS	Z	20	
A27	PA14	GPIO	I/O	DIS	Z	20	
B27	PA15	GPIO	I/O	DIS	Z	20	
C27	PA16	GPIO	I/O	DIS	Z	20	
D27	PA17	GPIO	I/O	DIS	Z	20	
E24	PA18	GPIO	I/O	DIS	Z	20	
E25	PA19	GPIO	I/O	DIS	Z	20	
E26	PA20	GPIO	I/O	DIS	Z	20	
E27	PA21	GPIO	I/O	DIS	Z	20	
F25	PA22	GPIO	I/O	DIS	Z	20	
F26	PA23	GPIO	I/O	DIS	Z	20	
F27	PA24	GPIO	I/O	DIS	Z	20	
F24	PA25	GPIO	I/O	DIS	Z	20	
G26	PA26	GPIO	I/O	DIS	Z	20	
G27	PA27	GPIO	I/O	DIS	Z	20	
F20,G20	VCC-PA	POWER	P	-	-	-	
GPIO B[7]							
B21	PB0	GPIO	I/O	DIS	Z	20	VCC-PB
C21	PB1	GPIO	I/O	DIS	Z	20	
A22	PB2	GPIO	I/O	DIS	Z	20	
B22	PB3	GPIO	I/O	DIS	Z	20	
C22	PB4	GPIO	I/O	DIS	Z	20	
D22	PB5	GPIO	I/O	DIS	Z	20	
B23	PB6	GPIO	I/O	DIS	Z	20	
D23	PB7	GPIO	I/O	DIS	Z	20	
G19	VCC-PB	POWER	P	-	-	-	
GPIO C[7]							
D2	PC0	GPIO	I/O	DIS	Z	20	VCC-PC
D4	PC1	GPIO	I/O	DIS	Z	20	
C3	PC2	GPIO	I/O	DIS	Z	20	
D5	PC3	GPIO	I/O	DIS	Pull-up	20	
C5	PC4	GPIO	I/O	DIS	Pull-up	20	
C4	PC5	GPIO	I/O	DIS	Z	20	

Ball#	Pin Name[1]	Default Function[2]	Type[3]	Default IO State[4]	Default Pull Up/Down[5]	Buffer Strength[6] (mA)	Power Supply
B1	PC6	GPIO	I/O	DIS	Pull-up	20	
B2	PC7	GPIO	I/O	DIS	Pull-up	20	
B3	PC8	GPIO	I/O	DIS	Z	20	
B4	PC9	GPIO	I/O	DIS	Z	20	
A1	PC10	GPIO	I/O	DIS	Z	20	
A2	PC11	GPIO	I/O	DIS	Z	20	
A3	PC12	GPIO	I/O	DIS	Z	20	
A4	PC13	GPIO	I/O	DIS	Z	20	
E4	PC14	GPIO	I/O	DIS	Z	20	
D3	PC15	GPIO	I/O	DIS	Z	20	
B5	PC16	GPIO	I/O	DIS	Z	20	
A5	PC17	GPIO	I/O	DIS	Z	20	
D6	PC18	GPIO	I/O	DIS	Z	20	
C6	PC19	GPIO	I/O	DIS	Z	20	
B6	PC20	GPIO	I/O	DIS	Z	20	
A6	PC21	GPIO	I/O	DIS	Z	20	
D7	PC22	GPIO	I/O	DIS	Z	20	
C7	PC23	GPIO	I/O	DIS	Z	20	
F7	PC24	GPIO	I/O	DIS	Z	20	
B7	PC25	GPIO	I/O	DIS	Pull-up	20	
A7	PC26	GPIO	I/O	DIS	Pull-up	20	
F6	PC27	GPIO	I/O	DIS	Pull-up	20	
G7,G8	VCC-PC	POWER	P	-	-	-	
GPIO D[7]							
T24	PD0	GPIO	I/O	DIS	Z	20	
T25	PD1	GPIO	I/O	DIS	Z	20	
U24	PD2	GPIO	I/O	DIS	Z	20	
U25	PD3	GPIO	I/O	DIS	Z	20	
V24	PD4	GPIO	I/O	DIS	Z	20	
V25	PD5	GPIO	I/O	DIS	Z	20	
W24	PD6	GPIO	I/O	DIS	Z	20	
W25	PD7	GPIO	I/O	DIS	Z	20	
Y24	PD8	GPIO	I/O	DIS	Z	20	
Y25	PD9	GPIO	I/O	DIS	Z	20	
W26	PD10	GPIO	I/O	DIS	Z	20	
W27	PD11	GPIO	I/O	DIS	Z	20	
Y26	PD12	GPIO	I/O	DIS	Z	20	
Y27	PD13	GPIO	I/O	DIS	Z	20	
AA26	PD14	GPIO	I/O	DIS	Z	20	
AA27	PD15	GPIO	I/O	DIS	Z	20	
AB26	PD16	GPIO	I/O	DIS	Z	20	

Ball#	Pin Name[1]	Default Function[2]	Type[3]	Default IO State[4]	Default Pull Up/Down[5]	Buffer Strength[6] (mA)	Power Supply
AB27	PD17	GPIO	I/O	DIS	Z	20	
AC26	PD18	GPIO	I/O	DIS	Z	20	
AC27	PD19	GPIO	I/O	DIS	Z	20	
AA25	PD20	GPIO	I/O	DIS	Z	20	
AA24	PD21	GPIO	I/O	DIS	Z	20	
AB25	PD22	GPIO	I/O	DIS	Z	20	
AB24	PD23	GPIO	I/O	DIS	Z	20	
AC24	PD24	GPIO	I/O	DIS	Z	20	
AD27	PD25	GPIO	I/O	DIS	Z	20	
AD26	PD26	GPIO	I/O	DIS	Z	20	
AD25	PD27	GPIO	I/O	DIS	Z	20	
V21,W21,W22	VCC-PD	POWER	P	-	-	-	
GPIO E[7]							
C12	PE0	GPIO	I/O	DIS	Z	20	
D13	PE1	GPIO	I/O	DIS	Z	20	
D14	PE2	GPIO	I/O	DIS	Z	20	
B13	PE3	GPIO	I/O	DIS	Z	20	
B14	PE4	GPIO	I/O	DIS	Z	20	
C13	PE5	GPIO	I/O	DIS	Z	20	
C14	PE6	GPIO	I/O	DIS	Z	20	
A13	PE7	GPIO	I/O	DIS	Z	20	
A14	PE8	GPIO	I/O	DIS	Z	20	
D15	PE9	GPIO	I/O	DIS	Z	20	
C15	PE10	GPIO	I/O	DIS	Z	20	
B15	PE11	GPIO	I/O	DIS	Z	20	
A15	PE12	GPIO	I/O	DIS	Z	20	
D16	PE13	GPIO	I/O	DIS	Z	20	
A16	PE14	GPIO	I/O	DIS	Z	20	
B16	PE15	GPIO	I/O	DIS	Z	20	
C16	PE16	GPIO	I/O	DIS	Z	20	
F18	VCC-PE	POWER	P	-	-	-	VCC-PE
GPIO F[7]							
E2	PF0	GPIO	I/O	DIS	Z	20	
E3	PF1	GPIO	I/O	DIS	Z	20	
E1	PF2	GPIO	I/O	DIS	Z	20	
D1	PF3	GPIO	I/O	DIS	Z	20	
C1	PF4	GPIO	I/O	DIS	Z	20	
C2	PF5	GPIO	I/O	DIS	Z	20	
G6	VCC-PF	POWER	P	-	-	-	VCC-PF
GPIO G[7]							
D17	PG0	GPIO	I/O	DIS	Z	20	VCC-PG

Ball#	Pin Name[1]	Default Function[2]	Type[3]	Default IO State[4]	Default Pull Up/Down[5]	Buffer Strength[6] (mA)	Power Supply
C17	PG1	GPIO	I/O	DIS	Z	20	
B17	PG2	GPIO	I/O	DIS	Z	20	
A17	PG3	GPIO	I/O	DIS	Z	20	
C18	PG4	GPIO	I/O	DIS	Z	20	
D18	PG5	GPIO	I/O	DIS	Z	20	
B18	PG6	GPIO	I/O	DIS	Z	20	
A18	PG7	GPIO	I/O	DIS	Z	20	
F19	PG8	GPIO	I/O	DIS	Z	20	
A19	PG9	GPIO	I/O	DIS	Z	20	
B19	PG10	GPIO	I/O	DIS	Z	20	
D19	PG11	GPIO	I/O	DIS	Z	20	
C19	PG12	GPIO	I/O	DIS	Z	20	
D20	PG13	GPIO	I/O	DIS	Z	20	
C20	PG14	GPIO	I/O	DIS	Z	20	
A20	PG15	GPIO	I/O	DIS	Z	20	
B20	PG16	GPIO	I/O	DIS	Z	20	
D21	PG17	GPIO	I/O	DIS	Z	20	
A21	PG18	GPIO	I/O	DIS	Z	20	
G18	VCC-PG	POWER	P	-	-	-	
GPIO H[7]							
D8	PH0	GPIO	I/O	DIS	Z	20	VCC-PH
C8	PH1	GPIO	I/O	DIS	Z	20	
B8	PH2	GPIO	I/O	DIS	Z	20	
A8	PH3	GPIO	I/O	DIS	Pull-up	20	
D9	PH4	GPIO	I/O	DIS	Pull-up	20	
C9	PH5	GPIO	I/O	DIS	Z	20	
B9	PH6	GPIO	I/O	DIS	Pull-up	20	
A9	PH7	GPIO	I/O	DIS	Pull-up	20	
D10	PH8	GPIO	I/O	DIS	Z	20	
F9	PH9	GPIO	I/O	DIS	Z	20	
F8	PH10	GPIO	I/O	DIS	Z	20	
G9	PH11	GPIO	I/O	DIS	Z	20	
G10	PH12	GPIO	I/O	DIS	Z	20	
C11	PH13	GPIO	I/O	DIS	Z	20	
B10	PH14	GPIO	I/O	DIS	Z	20	
A10	PH15	GPIO	I/O	DIS	Z	20	
D11	PH16	GPIO	I/O	DIS	Z	20	
C10	PH17	GPIO	I/O	DIS	Z	20	
B11	PH18	GPIO	I/O	DIS	Z	20	
A11	PH19	GPIO	I/O	DIS	Z	20	
D12	PH20	GPIO	I/O	DIS	Z	20	

Ball#	Pin Name[1]	Default Function[2]	Type[3]	Default IO State[4]	Default Pull Up/Down[5]	Buffer Strength[6] (mA)	Power Supply
G12	PH21	GPIO	I/O	DIS	Z	20	
F13	PH22	GPIO	I/O	DIS	Z	20	
G11	PH23	GPIO	I/O	DIS	Z	20	
F10	PH24	GPIO	I/O	DIS	Z	20	
G13	PH25	GPIO	I/O	DIS	Z	20	
F11	PH26	GPIO	I/O	DIS	Z	20	
G14	PH27	GPIO	I/O	DIS	Z	20	
F12	PH28	GPIO	I/O	DIS	Z	20	
F14	PH29	GPIO	I/O	DIS	Pull-up	20	
B12	PH30	GPIO	I/O	DIS	Pull-up	20	
G15，J14	VCC-PH	POWER	P	-	-	-	
GPIO L[7]							
P27	PL0	GPIO	I/O	DIS	Pull-up	20	VCC-RTC
R25	PL1	GPIO	I/O	DIS	Pull-up	20	
R24	PL2	GPIO	I/O	DIS	Z	20	
R22	PL3	GPIO	I/O	DIS	Z	20	
R26	PL4	GPIO	I/O	DIS	Z	20	
T21	PL5	GPIO	I/O	DIS	Z	20	
U21	PL6	GPIO	I/O	DIS	Z	20	
U22	PL7	GPIO	I/O	DIS	Z	20	
T22	PL8	GPIO	I/O	DIS	Z	20	
GPIO M[7]							
M26	PM0	GPIO	I/O	DIS	Z	20	VCC-PM
M27	PM1	GPIO	I/O	DIS	Z	20	
K21	PM2	GPIO	I/O	DIS	Z	20	
M22	PM3	GPIO	I/O	DIS	Z	20	
N24	PM4	GPIO	I/O	DIS	Z	20	
N25	PM5	GPIO	I/O	DIS	Z	20	
N26	PM6	GPIO	I/O	DIS	Z	20	
N27	PM7	GPIO	I/O	DIS	Z	20	
R19	VCC-PM	POWER	P	-	-	-	
System Control							
A12	UBOOT	-	I	-	Pull-up	-	VCC_PH
F17，G17	JTAG_SEL	-	I	-	Pull-up	-	VCC_PH
F16，G16	BOOT_SEL	-	I	-	Pull-up	-	VCC_PH
F15	TEST	-	I	-	Pull-down	-	VCC_PH
P19	VDDQE	-	P	-	-	-	
P24	NMI	-	I	I	Z	-	VCC_RTC
P25	RESET	-	I	I	Z	-	VCC_RTC
HDMI							
AF26	HTX0P	-	A	-	-	-	VCC-HDMI

Ball#	Pin Name[1]	Default Function[2]	Type[3]	Default IO State[4]	Default Pull Up/Down[5]	Buffer Strength[6] (mA)	Power Supply
AG26	HTX0N	-	A	-	-	-	
AF27	HTX1P	-	A	-	-	-	
AG27	HTX1N	-	A	-	-	-	
AE27	HTX2P	-	A	-	-	-	
AE26	HTX2N	-	A	-	-	-	
AF25	HTXCP	-	A	-	-	-	
AG25	HTXCN	-	A	-	-	-	
W19	VCC-HDMI	-	P	-	-	-	
AB21	HSCL	-	A	-	-	-	
AC25	HSDA	-	A	-	-	-	
AB22	HHPD	-	A	-	-	-	
USB							
T26	USB_DM0	-	A	-	-	-	
T27	USB_DP0	-	A	-	-	-	
U26	USB_DM1	-	A	-	-	-	
U27	USB_DP1	-	A	-	-	-	VCC-USB
V22	VCC-USB	-	P	-	-	-	
V26	USB_DM2	-	A	-	-	-	
V27	USB_DP2	-	A	-	-	-	
Touch Panel							
G22	TPX1	-	A	-	-	-	
N22	TPX2	-	A	-	-	-	AVCC
L21	TPY1	-	A	-	-	-	
J21	TPY2	-	A	-	-	-	
Audio Codec							
L27	PHOUTN	-	A	-	-	-	
L26	PHOUTP	-	A	-	-	-	
J24	PHINP	-	A	-	-	-	
J25	PHINN	-	A	-	-	-	
K27	HBIAS	-	A	-	-	-	
K26	MBIAS	-	A	-	-	-	
N21	MIC3N	-	A	-	-	-	
M21	MIC3P	-	A	-	-	-	
K25	MIC2N	-	A	-	-	-	AVCC
K24	MIC2P	-	A	-	-	-	
J26	MIC1N	-	A	-	-	-	
J27	MIC1P	-	A	-	-	-	
K22	VRA1	-	A	-	-	-	
J22	VRA2	-	A	-	-	-	
L22	AVCC	-	P	-	-	-	
H22	VRP	-	A	-	-	-	

Ball#	Pin Name[1]	Default Function[2]	Type[3]	Default IO State[4]	Default Pull Up/Down[5]	Buffer Strength[6] (mA)	Power Supply
L24	LINEOUTR	-	A	-	-	-	
L25	LINEOUTL	-	A	-	-	-	
H27	LINEINR	-	A	-	-	-	
H26	LINEINL	-	A	-	-	-	
J19	AGND	-	G	-	-	-	
H25	HPOUTR	-	A	-	-	-	
G25	HPCOMFB	-	A	-	-	-	
G24	HPCOM	-	A	-	-	-	
N19	HPBP	-	A	-	-	-	
G21	VCC-HP	-	P	-	-	-	
H24	HPOUTL	-	A	-	-	-	
LRADC							
M25	LRADC0	-	A	-	-	-	AVCC
M24	LRADC1	-	A	-	-	-	
MIPI DSI/CSI							
AD19	DSI-D0N	-	A	-	-	-	VCC-MIPI
AE19	DSI-D0P	-	A	-	-	-	
AD20	DSI-D1N	-	A	-	-	-	
AE20	DSI-D1P	-	A	-	-	-	
AD22	DSI-D2N	-	A	-	-	-	
AE22	DSI-D2P	-	A	-	-	-	
AD23	DSI-D3N	-	A	-	-	-	
AE23	DSI-D3P	-	A	-	-	-	
AD21	DSI-CKN	-	A	-	-	-	
AE21	DSI-CKP	-	A	-	-	-	
AF19	CSI2-D0N	-	A	-	-	-	
AG19	CSI2-D0P	-	A	-	-	-	
AF20	CSI2-D1N	-	A	-	-	-	
AG20	CSI2-D1P	-	A	-	-	-	
AF22	CSI2-D2N	-	A	-	-	-	
AG22	CSI2-D2P	-	A	-	-	-	
AF23	CSI2-D3N	-	A	-	-	-	
AG23	CSI2-D3P	-	A	-	-	-	
AF21	CSI2-CKN	-	A	-	-	-	
AG21	CSI2-CKP	-	A	-	-	-	
W16	VCC-MIPI	-	P	-	-	-	
RTC							
AG24	X24MI	-	A	-	-	-	VCC-RTC
AF24	X24MO	-	A	-	-	-	
T19	VIO-RTC	-	P	-	-	-	
R21	VCC-RTC	-	P	-	-	-	

Ball#	Pin Name[1]	Default Function[2]	Type[3]	Default IO State[4]	Default Pull Up/Down[5]	Buffer Strength[6] (mA)	Power Supply
Clock							
P26	X32KI	-	A	-	-	-	VCC-PLL
R27	X32KO	-	A	-	-	-	
V17	PLLTEST	-	A	-	-	-	
W18	PLLDV	-	P	-	-	-	
W17	PLL-VREG	-	P	-	-	-	
V19	VCC-PLL	-	P	-	-	-	
V18	GND-PLL	-	G	-	-	-	
Power							
P21，P22	VDD-CPUS	-	P	-	-	-	-
J15,J16,J17,J18,K15,K16,K17,K18,K19,L15,L16,L17,L18,L19,M15,M16,M17,M18,M19,N15,N16,N17,N18	VDD-CPU (23)	-	P	-	-	-	-
F21	CPU-VDDFB	-		-	-	-	-
H21	CPU-VDDSW	-		-	-	-	-
J9,J10,J11,K9,K10,K11,L9,L10,L11,M9,M10,M11	VDD-GPU (12)	-	P	-	-	-	-
T13,T14,T15,U13,U14,U15,V13,V14,V15,W13,W14,W15	VDD-SYS (12)	-	P	-	-	-	-
F22,J12,J13,K12,K13,K14,L12,L13,L14,M12,M13,M14,N9,N10,N11,N12,N13,N14,P9,P10,P11,P12,P13,P14,P15,P16,P17,P18,R9,R10,R11,R12,R13,R14,R15,R16,R17,R18,T11,T12,T16,T17,T18,U11,U12,U16,U17,U18,U19,V11,V12,V16,W11,W12,Y21,Y22,AA18,AA19,AA20,AA21,AA22,AB18,AB19,AB20,AD24,AE24,AE25	GND(67)	-	G	-	-	-	-

Table 5-1 Pin Characteristics

5.2. GPIO MULTIPLEXING FUNCTIONS

The following table provides a description of the A31 GPIO multiplexing functions.

Pin Name	Default Function	IO Type	Default IO State	Default Pull-up/ down	Function2	Function 3	Function 4	Function 5	Function 6
PA0	GPIO	I/O	DIS	Z	ETXD0	LCD1_D0	UART1_DTR	-	PA_EINT0
PA1		I/O	DIS	Z	ETXD1	LCD1_D1	UART1_DSR	-	PA_EINT1
PA2		I/O	DIS	Z	ETXD2	LCD1_D2	UART1_DCD	-	PA_EINT2
PA3		I/O	DIS	Z	ETXD3	LCD1_D3	UART1_RING	-	PA_EINT3
PA4		I/O	DIS	Z	ETXD4	LCD1_D4	UART1_TX	-	PA_EINT4
PA5		I/O	DIS	Z	ETXD5	LCD1_D5	UART1_RX	-	PA_EINT5
PA6		I/O	DIS	Z	ETXD6	LCD1_D6	UART1_RTS	-	PA_EINT6
PA7		I/O	DIS	Z	ETXD7	LCD1_D7	UART1_CTS	-	PA_EINT7
PA8		I/O	DIS	Z	ETXCLK	LCD1_D8	ECLK_IN0	-	PA_EINT8
PA9		I/O	DIS	Z	ETXEN	LCD1_D9	SDC3_CMD	SDC2_CMD	PA_EINT9

Pin Name	Default Function	IO Type	Default IO State	Default Pull-up/ down	Function2	Function 3	Function 4	Function 5	Function 6
PA10		I/O	DIS	Z	EGTXCLK	LCD1_D10	SDC3_CLK	SDC2_CLK	PA_EINT10
PA11		I/O	DIS	Z	ERXD0	LCD1_D11	SDC3_D0	SDC2_D0	PA_EINT11
PA12		I/O	DIS	Z	ERXD1	LCD1_D12	SDC3_D1	SDC2_D1	PA_EINT12
PA13		I/O	DIS	Z	ERXD2	LCD1_D13	SDC3_D2	SDC2_D2	PA_EINT13
PA14		I/O	DIS	Z	ERXD3	LCD1_D14	SDC3_D3	SDC2_D3	PA_EINT14
PA15		I/O	DIS	Z	ERXD4	LCD1_D15	CLKA_OUT	-	PA_EINT15
PA16		I/O	DIS	Z	ERXD5	LCD1_D16	DMIC_CLK	-	PA_EINT16
PA17		I/O	DIS	Z	ERXD6	LCD1_D17	DMIC_DIN	-	PA_EINT17
PA18		I/O	DIS	Z	ERXD7	LCD1_D18	CLKB_OUT	-	PA_EINT18
PA19		I/O	DIS	Z	ERXDV	LCD1_D19	PWM3_P	-	PA_EINT19
PA20		I/O	DIS	Z	ERXCLK	LCD1_D20	PWM3_N	-	PA_EINT20
PA21		I/O	DIS	Z	ETXERR	LCD1_D21	SPI3_CS0	-	PA_EINT21
PA22		I/O	DIS	Z	ERXERR	LCD1_D22	SPI3_CLK	-	PA_EINT22
PA23		I/O	DIS	Z	ECOL	LCD1_D23	SPI3_MOSI	-	PA_EINT23
PA24		I/O	DIS	Z	ECRS	LCD1_CLK	SPI3_MISO	-	PA_EINT24
PA25		I/O	DIS	Z	ECLKIN	LCD1_DE	SPI3_CS1	-	PA_EINT25
PA26		I/O	DIS	Z	EMDC	LCD1_HSYNC	CLKC_OUT	-	PA_EINT26
PA27		I/O	DIS	Z	EMDIO	LCD1_VSYNC	ECLK_IN1	-	PA_EINT27
PB0	GPIO	I/O	DIS	Z	I2S0_MCLK	UART3_CTS	MCS_MCLK1	-	PB_EINT0
PB1		I/O	DIS	Z	I2S0_BCLK	-	-	-	PB_EINT1
PB2		I/O	DIS	Z	I2S0_LRCK	-	-	-	PB_EINT2
PB3		I/O	DIS	Z	I2S0_DO0	-	-	-	PB_EINT3
PB4		I/O	DIS	Z	I2S0_DO1	UART3_RTS	-	-	PB_EINT4
PB5		I/O	DIS	Z	I2S0_DO2	UART3_TX	TWI3_SCK	-	PB_EINT5
PB6		I/O	DIS	Z	I2S0_DO3	UART3_RX	TWI3_SDA	-	PB_EINT6
PB7		I/O	DIS	Z	I2S0_DI	-	-	-	PB_EINT7
PC0	GPIO	I/O	DIS	Z	NAND0_WE	SPI0_MOSI	-	-	-
PC1		I/O	DIS	Z	NAND0_ALE	SPI0_MISO	-	-	-
PC2		I/O	DIS	Z	NAND0_CLE	SPI0_CLK	-	-	-
PC3		I/O	DIS	Pull-up	NAND0_CE1	-	-	-	-
PC4		I/O	DIS	Pull-up	NAND0_CE0	-	-	-	-
PC5		I/O	DIS	Z	NAND0_RE	-	-	-	-
PC6		I/O	DIS	Pull-up	NAND0_RB0	SDC2_CMD	SDC3_CMD	-	-
PC7		I/O	DIS	Pull-up	NAND0_RB1	SDC2_CLK	SDC3_CLK	-	-
PC8		I/O	DIS	Z	NAND0_DQ0	SDC2_D0	SDC3_D0	-	-
PC9		I/O	DIS	Z	NAND0_DQ1	SDC2_D1	SDC3_D1	-	-
PC10		I/O	DIS	Z	NAND0_DQ2	SDC2_D2	SDC3_D2	-	-
PC11		I/O	DIS	Z	NAND0_DQ3	SDC2_D3	SDC3_D3	-	-
PC12		I/O	DIS	Z	NAND0_DQ4	SDC2_D4	SDC3_D4	-	-
PC13		I/O	DIS	Z	NAND0_DQ5	SDC2_D5	SDC3_D5	-	-
PC14		I/O	DIS	Z	NAND0_DQ6	SDC2_D6	SDC3_D6	-	-

Pin Name	Default Function	IO Type	Default IO State	Default Pull-up/ down	Function2	Function 3	Function 4	Function 5	Function 6
PC15		I/O	DIS	Z	NAND0_DQ7	SDC2_D7	SDC3_D7	-	-
PC16		I/O	DIS	Z	NAND0_DQ8	NAND1_DQ0	TRACE_DOUT 0	-	-
PC17		I/O	DIS	Z	NAND0_DQ9	NAND1_DQ1	TRACE_DOUT 1	-	-
PC18		I/O	DIS	Z	NAND0_DQ10	NAND1_DQ2	TRACE_DOUT 2	-	-
PC19		I/O	DIS	Z	NAND0_DQ11	NAND1_DQ3	TRACE_DOUT 3	-	-
PC20		I/O	DIS	Z	NAND0_DQ12	NAND1_DQ4	TRACE_DOUT 4	-	-
PC21		I/O	DIS	Z	NAND0_DQ13	NAND1_DQ5	TRACE_DOUT 5	-	-
PC22		I/O	DIS	Z	NAND0_DQ14	NAND1_DQ6	TRACE_DOUT 6	-	-
PC23		I/O	DIS	Z	NAND0_DQ15	NAND1_DQ7	TRACE_DOUT 7	-	-
PC24		I/O	DIS	Z	NAND0_DQS	SDC2_RST	SDC3_RST	-	-
PC25		I/O	DIS	Pull-up	NAND0_CE2	-	-	-	-
PC26		I/O	DIS	Pull-up	NAND0_CE3	-	-	-	-
PC27		I/O	DIS	Pull-up	-	SPI0_CS0	-	-	-
PD0	GPIO	I/O	DIS	Z	LCD0_D0	LVDS0_VP0	-	-	-
PD1		I/O	DIS	Z	LCD0_D1	LVDS0_VN0	-	-	-
PD2		I/O	DIS	Z	LCD0_D2	LVDS0_VP1	-	-	-
PD3		I/O	DIS	Z	LCD0_D3	LVDS0_VN1	-	-	-
PD4		I/O	DIS	Z	LCD0_D4	LVDS0_VP2	-	-	-
PD5		I/O	DIS	Z	LCD0_D5	LVDS0_VN2	-	-	-
PD6		I/O	DIS	Z	LCD0_D6	LVDS0_VPC	-	-	-
PD7		I/O	DIS	Z	LCD0_D7	LVDS0_VNC	-	-	-
PD8		I/O	DIS	Z	LCD0_D8	LVDS0_VP3	-	-	-
PD9		I/O	DIS	Z	LCD0_D9	LVDS0_VN3	-	-	-
PD10		I/O	DIS	Z	LCD0_D10	LVDS1_VP0	-	-	-
PD11		I/O	DIS	Z	LCD0_D11	LVDS1_VN0	-	-	-
PD12		I/O	DIS	Z	LCD0_D12	LVDS1_VP1	-	-	-
PD13		I/O	DIS	Z	LCD0_D13	LVDS1_VN1	-	-	-
PD14		I/O	DIS	Z	LCD0_D14	LVDS1_VP2	-	-	-
PD15		I/O	DIS	Z	LCD0_D15	LVDS1_VN2	-	-	-
PD16		I/O	DIS	Z	LCD0_D16	LVDS1_VPC	-	-	-
PD17		I/O	DIS	Z	LCD0_D17	LVDS1_VNC	-	-	-
PD18		I/O	DIS	Z	LCD0_D18	LVDS1_VP3	-	-	-
PD19		I/O	DIS	Z	LCD0_D19	LVDS1_VN3	-	-	-
PD20		I/O	DIS	Z	LCD0_D20	-	-	-	-
PD21		I/O	DIS	Z	LCD0_D21	-	-	-	-
PD22		I/O	DIS	Z	LCD0_D22	-	-	-	-
PD23		I/O	DIS	Z	LCD0_D23	-	-	-	-
PD24		I/O	DIS	Z	LCD0_CLK	-	-	-	-
PD25		I/O	DIS	Z	LCD0_DE	-	-	-	-
PD26		I/O	DIS	Z	LCD0_HSYNC	-	-	-	-
PD27		I/O	DIS	Z	LCD0_VSYNC	-	-	-	-

Pin Name	Default Function	IO Type	Default IO State	Default Pull-up/ down	Function2	Function 3	Function 4	Function 5	Function 6
PE0	GPIO	I/O	DIS	Z	CSI_PCLK	TS_CLK	-	-	PE_EINT0
PE1		I/O	DIS	Z	CSI_MCLK	TS_ERR	-	-	PE_EINT1
PE2		I/O	DIS	Z	CSI_HSYNC	TS_SYNC	-	-	PE_EINT2
PE3		I/O	DIS	Z	CSI_VSYNC	TS_DVLD	-	-	PE_EINT3
PE4		I/O	DIS	Z	CSI_D0	UART5_TX	-	-	PE_EINT4
PE5		I/O	DIS	Z	CSI_D1	UART5_RX	-	-	PE_EINT5
PE6		I/O	DIS	Z	CSI_D2	UART5_RTS		-	PE_EINT6
PE7		I/O	DIS	Z	CSI_D3	UART5_CTS	-	-	PE_EINT7
PE8		I/O	DIS	Z	CSI_D4	TS_D0	-	-	PE_EINT8
PE9		I/O	DIS	Z	CSI_D5	TS_D1	-	-	PE_EINT9
PE10		I/O	DIS	Z	CSI_D6	TS_D2	-	-	PE_EINT10
PE11		I/O	DIS	Z	CSI_D7	TS_D3	-	-	PE_EINT11
PE12		I/O	DIS	Z	CSI_D8	TS_D4	-	-	PE_EINT12
PE13		I/O	DIS	Z	CSI_D9	TS_D5	-	-	PE_EINT13
PE14		I/O	DIS	Z	CSI_D10	TS_D6	-	-	PE_EINT14
PE15		I/O	DIS	Z	CSI_D11	TS_D7	-	-	PE_EINT15
PE16		I/O	DIS	Z	MCS_MCLK1	-	-	-	PE_EINT16
PF0	GPIO	I/O	DIS	Z	SDC0_D1	-	JTAG_MS1	-	-
PF1		I/O	DIS	Z	SDC0_D0	-	JTAG_DI1	-	-
PF2		I/O	DIS	Z	SDC0_CLK	-	UART0_TX	-	-
PF3		I/O	DIS	Z	SDC0_CMD	-	JTAG_DO1	-	-
PF4		I/O	DIS	Z	SDC0_D3	-	UART0_RX	-	-
PF5		I/O	DIS	Z	SDC0_D2	-	JTAG_CK1	-	-
PG0	GPIO	I/O	DIS	Z	SDC1_CLK	-	-	-	PG_EINT0
PG1		I/O	DIS	Z	SDC1_CMD	-	-	-	PG_EINT1
PG2		I/O	DIS	Z	SDC1_D0	-	-	-	PG_EINT2
PG3		I/O	DIS	Z	SDC1_D1	-	-	-	PG_EINT3
PG4		I/O	DIS	Z	SDC1_D2	-	-	-	PG_EINT4
PG5		I/O	DIS	Z	SDC1_D3	-	-	-	PG_EINT5
PG6		I/O	DIS	Z	UART2_TX	-	-	-	PG_EINT6
PG7		I/O	DIS	Z	UART2_RX	-	-	-	PG_EINT7
PG8		I/O	DIS	Z	UART2_RTS	-	-	-	PG_EINT8
PG9		I/O	DIS	Z	UART2_CTS	-	-	-	PG_EINT9
PG10		I/O	DIS	Z	TWI3_SCK	USB_DP3	-	-	PG_EINT10
PG11		I/O	DIS	Z	TWI3_SDA	USB_DM3	-	-	PG_EINT11
PG12		I/O	DIS	Z	SPI1_CS1	I2S1_MCLK	-	-	PG_EINT12
PG13		I/O	DIS	Z	SPI1_CS0	I2S1_BCLK	-	-	PG_EINT13
PG14		I/O	DIS	Z	SPI1_CLK	I2S1_LRCK	-	-	PG_EINT14
PG15		I/O	DIS	Z	SPI1_MOSI	I2S1_DIN	-	-	PG_EINT15
PG16		I/O	DIS	Z	SPI1_MISO	I2S1_DOUT	-	-	PG_EINT16
PG17		I/O	DIS	Z	UART4_TX	-	-	-	PG_EINT17

Pin Name	Default Function	IO Type	Default IO State	Default Pull-up/ down	Function2	Function 3	Function 4	Function 5	Function 6
PG18		I/O	DIS	Z	UART4_RX	-	-	-	PG_EINT18
PH0	GPIO	I/O	DIS	Z	NAND1_WE	-	TRACE_DOUT 8	-	-
PH1		I/O	DIS	Z	NAND1_ALE	-	TRACE_DOUT 9	-	-
PH2		I/O	DIS	Z	NAND1_CLE	-	TRACE_DOUT 10	-	-
PH3		I/O	DIS	Pull-up	NAND1_CE1	-	TRACE_DOUT 11	-	-
PH4		I/O	DIS	Pull-up	NAND1_CE0	-	TRACE_DOUT 12	-	-
PH5		I/O	DIS	Z	NAND1_RE	-	TRACE_DOUT 13	-	-
PH6		I/O	DIS	Pull-up	NAND1_RB0	-	TRACE_DOUT 14	-	-
PH7		I/O	DIS	Pull-up	NAND1_RB1	-	TRACE_DOUT 15	-	-
PH8		I/O	DIS	Z	NAND1_DQS	-	TRACE_CLK	-	-
PH9		I/O	DIS	Z	SPI2_CS0	JTAG_MS0	PWM1_P	-	-
PH10		I/O	DIS	Z	SPI2_CLK	JTAG_CK0	PWM1_N	-	-
PH11		I/O	DIS	Z	SPI2_MOSI	JTAG_DO0	PWM2_P	-	-
PH12		I/O	DIS	Z	SPI2_MISO	JTAG_DI0	PWM2_N	-	-
PH13		I/O	DIS	Z	PWM0	-	-	-	-
PH14		I/O	DIS	Z	TWI0_SCK	-	-	-	-
PH15		I/O	DIS	Z	TWI0_SDA	-	-	-	-
PH16		I/O	DIS	Z	TWI1_SCK	-	-	-	-
PH17		I/O	DIS	Z	TWI1_SDA	-	-	-	-
PH18		I/O	DIS	Z	TWI2_SCK	-	-	-	-
PH19		I/O	DIS	Z	TWI2_SDA	-	-	-	-
PH20		I/O	DIS	Z	UART0_TX	-	-	-	-
PH21		I/O	DIS	Z	UART0_RX	-	-	-	-
PH22		I/O	DIS	Z	-	-	-	-	-
PH23		I/O	DIS	Z	-	-	-	-	-
PH24		I/O	DIS	Z	-	-	-	-	-
PH25		I/O	DIS	Z	-	-	-	-	-
PH26		I/O	DIS	Z	-	-	-	-	-
PH27		I/O	DIS	Z	-	-	-	-	-
PH28		I/O	DIS	Z	-	-	TRACE_CTL	-	-
PH29		I/O	DIS	Pull-up	NAND1_CE2	-	-	-	-
PH30		I/O	DIS	Pull-up	NAND1_CE3	-	-	-	-
PL0	GPIO	I/O	DIS	Pull-up	S_TWI_SCK	S_P2WI_SCK	-	-	-
PL1		I/O	DIS	Pull-up	S_TWI_SDA	S_P2WI_SDA	-	-	-
PL2		I/O	DIS	Z	S_UART_TX	-	-	-	-
PL3		I/O	DIS	Z	S_UART_RX	-	-	-	-
PL4		I/O	DIS	Z	S_IR_RX	-	-	-	-
PL5		I/O	DIS	Z	S_PL_EINT0	S_JTAG_MS	-	-	-
PL6		I/O	DIS	Z	S_PL_EINT1	S_JTAG_CK	-	-	-
PL7		I/O	DIS	Z	S_PL_EINT2	S_JTAG_DO	-	-	-
PL8		I/O	DIS	Z	S_PL_EINT3	S_JTAG_DI	-	-	-

Pin Name	Default Function	IO Type	Default IO State	Default Pull-up/ down	Function2	Function 3	Function 4	Function 5	Function 6
PM0	GPIO	I/O	DIS	Z	S_PM_EINT0	-	-	-	-
PM1		I/O	DIS	Z	S_PM_EINT1	-	-	-	-
PM2		I/O	DIS	Z	S_PM_EINT2	1WIRE	-	-	-
PM3		I/O	DIS	Z	S_PM_EINT3	-	-	-	-
PM4		I/O	DIS	Z	S_PM_EINT4	-	-	-	-
PM5		I/O	DIS	Z	S_PM_EINT5	-	-	-	-
PM6		I/O	DIS	Z	S_PM_EINT6	-	-	-	-
PM7		I/O	DIS	Z	S_PM_EINT7	RTC_CLKO	-	-	-

Table 5-2 Multiplexing Functions

5.3. DETAILED PIN/SIGNAL DESCRIPTION

Following table describes the 609 pins of A31.

Pin/Signal Name	Description	Type
DRAM		
S0DQ[31:0]	DRAM0 Data Input/Output DQ[31:0]	I/O
S0DQS[3:0]	DRAM0 Data Strobe DQS[3:0]	I/O
S0DQSB[3:0]	DRAM0 Data Strobe DQSB[3:0]	I/O
S0DQM[3:0]	DRAM0 DQ Mask [3:0]	O
S0CK	DRAM0 Clock (Positive)	O
S0CKB	DRAM0 Clock (Negative)	O
S0CKE[1:0]	DRAM0 Clock Enable [1:0]	O
S0A[15:0]	DRAM0 data Address [15:0]	O
S0WE	DRAM0 Write Enable	O
S0CAS	DRAM0 Column Address Strobe	O
S0RAS	DRAM0 Row Address Strobe	O
S0CS[1:0]	DRAM0 Chip Select [1:0]	O
S0BA[2:0]	DRAM0 Bank Address [2:0]	O
S0ODT[1:0]	DRAM0 On Die Termination [1:0]	O
S0RST	DRAM0 Reset	O
S0ZQ	DRAM0 ZQ Calibration	A
S0VREF	DRAM0 Reference Input	P
VCC-DRAM	DRAM Power Supply	P
GND-DRAM	DRAM Ground	G
VDD-DLL	DLL Power Supply	P
S0ADBG	DRAM0 Analog Debug	A
S0DDBG0	DRAM0 Digital DBG0	A
S0DDBG1	DRAM0 Digital DBG1	A
S1DQ[31:0]	DRAM1 Data Input/Output DQ[31:0]	I/O
S1DQS[3:0]	DRAM1 Data Strobe DQS[3:0]	I/O
S1DQSB[3:0]	DRAM1 Data Strobe DQSB[3:0]	I/O

Pin/Signal Name	Description	Type
S1DQM[3:0]	DRAM1 DQ Mask [3:0]	O
S1CK	DRAM1 Clock (Positive)	O
S1CKB	DRAM1 Clock (Negative)	O
S1CKE[1:0]	DRAM1 Clock Enable	O
S1A[15:0]	DRAM1 Address[15:0]	O
S1WE	DRAM1 Write Enable	O
S1CAS	DRAM1 Column Address Strobe	O
S1RAS	DRAM1 Row Address Strobe	O
S1CS[1:0]	DRAM1 Chip Select[1:0]	O
S1BA[2:0]	DRAM1 Bank Address[2:0]	O
S1ODT[1:0]	DRAM1 On Die Termination [1:0]	O
S1RST	DRAM1 Reset	O
S1ZQ	DRAM1 ZQ Calibration	A
S1VREF	DRAM1 Reference Input	P
S1ADGB	DRAM1 Analog Debug	A
S1DDBG0	DRAM1 Digital Debug0	A
S1DDBG1	DRAM1 Digital Debug1	A
GPIO		
PA[27:0]	GPIO A Bit [27:0]	I/O
VCC-PA	GPIO A Power Supply	P
PB[7:0]	GPIO B Bit [7:0]	I/O
VCC-PB	GPIO B Power Supply	P
PC[27:0]	GPIO C Bit [27:0]	I/O
VCC-PC	GPIO C Power Supply	P
PD[27:0]	GPIO D Bit [27:0]	I/O
VCC-PD	GPIO D Power Supply	P
PE[16:0]	GPIO E Bit [16:0]	I/O
VCC-PE	GPIO E Power Supply	P
PF[5:0]	GPIO F Bit [5:0]	I/O
VCC-PF	GPIO F Power Supply	P
PG[18:0]	GPIO G Bit [18:0]	I/O
VCC-PG	GPIO G Power Supply	P
PH[30:0]	GPIO H Bit[30:0]	I/O
VCC-PH	GPIO H Power Supply	P
PL[8:0]	GPIO L Bit [8:0]	I/O
PM[7:0]	GPIO M Bit [7:0]	I/O
VCC-PM	GPIO M Power Supply	P
System Control		
UBOOT	UBOOT	I
JTAG_SEL	JTAG Mode Select	I
BOOT_SEL	BOOT Mode Select	I
TEST	TEST Signal	I

Pin/Signal Name	Description	Type
VDDQE	eFUSE Power Supply	P
NMI	Non-Maskable Interrupt	I
RESET	RESET Signal	I
HDMI		
HTX0P	TMSD Data 0 Positive	A
HTX0N	TMSD Data 0 Negative	A
HTX1P	TMSD Data 1 Positive	A
HTX1N	TMSD Data 1 Negative	A
HTX2P	TMSD Data 2 Positive	A
HTX2N	TMSD Data 2 Negative	A
HTXCP	TMSD Clock Positive	A
HTXCN	TMSD Clock Negative	A
VCC-HDMI	HDMI Power Supply	P
HSCL	HDMI DDC Clock	A
HSDA	HDMI DDC Data	A
HHPD	HDMI Hot Plug Detection signal	A
USB		
USB_DM0	USB DM0 Signal	A
USB_DP0	USB DP0 Signal	A
USB_DM1	USB DM1 Signal	A
USB_DP1	USB DP1 Signal	A
VCC-USB	USB Power Supply	P
USB_DM2	USB DM2 Signal	A
USB_DP2	USB DP2 Signal	A
USB_DP3	USB DP3 Signal	A
USB_DM3	USB DM3 Signal	A
TP		
TPX1	Touch Panel ADC Input	A
TPX2	Touch Panel ADC Input	A
TPY1	Touch Panel ADC Input	A
TPY2	Touch Panel ADC Input	A
Audio Codec		
PHOUTN	Phone Negative Output	A
PHOUTP	Phone Positive Output	A
PHINP	Phone Positive Input	A
PHINN	Phone Negative Input	A
HBIAS	Headphone Microphone Bias	A
MBIAS	Master Analog Microphone Bias	A
MIC3N	MIC Negative Input 3	A
MIC3P	MIC Positive Input 3	A
MIC2N	MIC Negative Input 2	A
MIC2P	MIC Positive Input 2	A

Pin/Signal Name	Description	Type
MIC1N	MIC Negative Input 1	A
MIC1P	MIC Positive Input 1	A
VRA1	Reference (1.5 V)	A
VRA2	Reference (1.5 V)	A
AVCC	Analog Power Supply	P
VRP	Reference (3.0 V)	A
LINEOUTR	LINE-OUT Right Channel Output	A
LINEOUTL	LINE-OUT Left Channel Output	A
LINEINR	LINE-IN Right Channel Input	A
LINEINL	LINE-IN Left Channel Input	A
AGND	Analog Ground	G
HPOUTR	Headphone Right Channel Output	A
HPCOMFB	Headphone Common Reference Feedback	A
HPCOM	Headphone Common Reference	A
HPBP	Headphone Bypass Output	A
VCC-HP	Headphone Power Supply	P
HPOUTL	Headphone Left Channel Output	A
LRADC		
LRADC0	LRADC input0	A
LRADC1	LRADC input1	A
MIPI DSI/CSI		
DSI_D0N	MIPI DSI Data 0 Negative	A
DSI_D0P	MIPI DSI Data 0 Positive	A
DSI_D1N	MIPI DSI Data 1 Negative	A
DSI_D1P	MIPI DSI Data 1 Positive	A
DSI_D2N	MIPI DSI Data 2 Negative	A
DSI_D2P	MIPI DSI Data 2 Positive	A
DSI_D3N	MIPI DSI Data 3 Negative	A
DSI_D3P	MIPI DSI Data 3 Positive	A
DSI-CKN	MIPI DSI Clock Negative	A
DSI-CKP	MIPI DSI Clock Positive	A
CSI_DN0	MIPI CSI Data 0 Negative	A
CSI_DP0	MIPI CSI Data 0 Positive	A
CSI_DN1	MIPI CSI Data 1 Negative	A
CSI_DP1	MIPI CSI Data 1 Positive	A
CSI_DN2	MIPI CSI Data 2 Negative	A
CSI_DP2	MIPI CSI Data 2 Positive	A
CSI_DN3	MIPI CSI Data 3 Negative	A
CSI_DP3	MIPI CSI Data 3 Positive	A
CSI-CKN	MIPI CSI Clock Negative	A
CSI-CKP	MIPI CSI Clock Positive	A
VCC-MIPI	MIPI Power Supply	P

Pin/Signal Name	Description	Type
RTC		
VIO-RTC	RTC Digital Power	P
VCC-RTC	RTC Power Supply	P
Clock		
X24MI	Clock Input Of 24MHz Crystal	A
X24MO	Clock Output Of 24MHz Crystal	A
X32KI	Clock Input Of 32768Hz Crystal	A
X32KO	Clock Output Of 32768Hz Crystal	A
PLLTEST	PLL Test Signal	A
PLLDV	PLL Power	P
PLL-VREG	PLL Power	P
VCC-PLL	PLL Power Supply	P
GND-PLL	PLL Ground	G
SD (x=[3:0])		
SDCx_CMD	SDx/MMCx/SDIOx Command Signal	I/O
SDCx_CLK	SDx/MMCx/SDIOx Clock	O
SDC0_D[3:0]	SD0/MMC0/SDIO0 Data [3:0]	I/O
SDC1_D[3:0]	SD1/MMC1/SDIO1 Data [3:0]	I/O
SDC2_D[7:0]	SD2/MMC2/SDIO2 Data [7:0]	I/O
SDC3_D[7:0]	SD3/MMC3/SDIO3 Data [7:0]	I/O
SDC2_RST	SD2/MMC2/SDIO2 Reset Signal	I/O
SDC3_RST	SD3/MMC3/SDIO3 Reset Signal	I/O
NAND (x=[1:0])		
NAND0_DQ[15:0]	NAND Flash0 Data Bit [15:0]	I/O
NAND1_DQ[7:0]	NAND Flash1 Data Bit [7:0]	I/O
NANDx_DQS	NADN Flash Data Strobe	I/O
NANDx_WE	NAND Flash Write Enable	O
NANDx_RE	NAND Flash chip Read Enable	O
NANDx_ALE	NAND Flash Address Latch Enable	O
NANDx_CLE	NAND Command Latch Enable	O
NANDx_CE[3:0]	NAND Flash Chip Select [3:0]	O
NANDx_RB[1:0]	NAND Flash Ready/Busy Bit	I
JTAG		
S_JTAG_MS	N/A	I/O
S_JTAG_CK	N/A	I/O
S_JTAG_DO	N/A	I/O
S_JTAG_DI	N/A	I/O
JTAG_MS[1:0]	N/A	I/O
JTAG_CK[1:0]	N/A	I/O
JTAG_DO[1:0]	N/A	I/O
JTAG_DI[1:0]	N/A	I/O
ETM TRACE		

Pin/Signal Name	Description	Type
TRACE_DOUT[15:0]	ETM TRACE Port Data Output	I/O
TRACE_CLK	ETM TRACE Port Clock	I/O
TRACE_CTL	ETM TRACE Port Control	I/O
Interrupt		
PA_EINT[27:0]	GPIO A Interrupt	I/O
PB_EINT[7:0]	GPIO B Interrupt	I/O
PE_EINT[16:0]	GPIO E Interrupt	I/O
S_PL_EINT[3:0]	GPIO L Interrupt	I/O
S_PM_EINT[7:0]	GPIO M Interrupt	I/O
PWM (x=[3:1])		
PWMx_P	PWM Output Positive	I/O
PWMx_N	PWM Output Negative	I/O
PWM0	PWM 0	I/O
IR		
S_IR_RX	IR Data Receive	I
LCD (x=[1:0])		
LCD0_D[23:0]	LCD0 Data Bit [23:0]	O
LCD1_D[23:0]	LCD1 Data Bit [23:0]	O
LCDx_CLK	LCD Clock signal	O
LCDx_DE	LCD Data Enable	O
LCDx_HSYNC	LCD Horizontal SYNC	O
LCDx_VSYNC	LCD Vertical SYNC	O
LVDS		
LVDS0_VP[3:0]	LVDS Channel 0 Data Positive Signal Output[3:0]	A
LVDS0_VN[3:0]	LVDS Channel 0 Data Negative Signal Output[3:0]	A
LVDS0_VPC	LVDS Channel 0 Clock Positive Signal Output	A
LVDS0_VNC	LVDS Channel 0 Clock Negative Signal Output	A
LVDS1_VP[3:0]	LVDS Channel 1 Data Positive Signal Output[3:0]	A
LVDS1_VN[3:0]	LVDS Channel 1 Data Negative Signal Output[3:0]	A
LVDS1_VPC	LVDS Channel 1 Clock Positive Signal Output	A
LVDS1_VNC	LVDS Channel 1 Clock Negative Signal Output	A
I2S (x=[1:0])		
I2Sx_MCLK	I2S Master Clock (system clock)	O
I2Sx_BCLK	I2S Bit Clock	I/O
I2Sx_LRCK	I2S Left/Right Channel Select Clock	I/O
I2S1_DIN	I2S1 Data Input	I
I2S1_DOUT	I2S1 Data Output	O
I2S0_DO[3:0]	I2S0 Data Output	O
I2S0_DI	I2S0 Data Input	I
CSI		
CSI_PCLK	CSI Pixel Clock	I
CSI_MCLK	CSI Master Clock	O

Pin/Signal Name	Description	Type
CSI_HSYNC	CSI Horizontal SYNC	I
CSI_VSYNC	CSI Vertical SYNC	I
CSI_D[11:0]	CSI Data bit [11:0]	I
MCS_MCLK1	Master Clock for MIPI CSI	O
TS		
TS_CLK	Transport Stream Clock	I
TS_ERR	Transport Stream Error Indicate	I
TS_SYNC	Transport Stream SYNC	I
TS_DVLD	Transport Stream Valid Signal	I
TS_D[7:0]	Transport Stream Data	I
EMAC		
ETXD[7:0]	EMAC MII Transmit Data Nibble Data Bit[7:0]	O
ETXCLK	EMAC MII Transmit Clock	O
ETXEN	EMAC MII Transmit Enable	O
EGTXCLK	EMAC TCLK signal	O
ERXD[7:0]	EMAC MII Receive Data Nibble Data Bit[7:0]	I
ERXDV	EMAC MII Receive Data Valid	I
ERXCLK	EMAC MII Receive Clock	I
ETXERR	EMAC MII Transmit Error	O
ERXERR	EMAC MII Receive Error	I
ECOL	EMAC MII Collision Detect	I
ECRS	EMAC MII Carrier Sense	I
ECLKIN	EMAC Clock Input	I
EMDC	EMAC MII Management Data Clock	O
EMDIO	EMAC MII Management Data Input/Output	I/O
ECLK_IN0	EMAC Clock Input	I
ECLK_IN1	EMAC Clock Input	I
SPI (x=[3:0])		
SPI0_CS0	SPI0 Chip Select signal 0	I/O
SPI1_CS[1:0]	SPI1 Chip Select signal[1:0]	I/O
SPI2_CS0	SPI2 Chip Select signal 0	I/O
SPI3_CS[1:0]	SPI3 Chip Select signal [1:0]	I/O
SPIx_CLK	SPI Clock signal	I/O
SPIx_MOSI	SPI Master data Out, Slave data In	I/O
SPIx_MISO	SPI Master data In, Slave data Out	I/O
UART (x=[5:0])		
UART1_DTR	UART Data Terminal Ready	O
UART1_DSR	UART Data Set Ready	I
UART1_DCD	UART Data Carrier Detect	I
UART1_RING	UART RING indicator	I
UARTx_CTS	UART Data Clear To Send	I
UARTx_RTS	UART Data Request To Send	O

Pin/Signal Name	Description	Type
UARTx_TX[5:0]	UART Data Transmit	O
UARTx_RX[5:0]	UART Data Receive	I
S_UART_TX	UART Data Transmit	O
S_UART_RX	UART Data Receive	I
TWI (x=[3:0])		
TWIx_SCK	TWI Serial Clock Signal	I/O
TWIx_SDA	TWI Serial Data Signal	I/O
S_TWI_SCK	TWI Serial Clock Signal	I/O
S_TWI_SDA	TWI Serial Data Signal	I/O
S_P2WI_SCK	P2WI Serial Clock Signal	I/O
S_P2WI_SDA	P2WI Serial Data Signal	I/O
Others		
CLKA_OUT	CLOCK OUT A	O
CLKB_OUT	CLOCK OUT B	O
CLKC_OUT	CLOCK OUT C	O
CK32KO	32K Crystal Clock Output	O
RTC_CLKO	RTC Clock Output	O
1WIRE	One WIRE signal	I/O

Table 5-3 Detailed Pin Description

5.4. POWER/GND SIGNAL DESCRIPTION

NOTES

1) VRP/VRA1/VRA2 are output type, and are not for third party development use.

Signal Name	Description	Ball#
HDMI		
VCC-HDMI	HDMI Power Supply	W19
USB Power		
VCC-USB	USB Power Supply	V22
Clock		
VCC-PLL	PLL Power Supply	V19
GND-PLL	PLL Ground	V18
MIPI		
VCC-MIPI	MIPI Power Supply	W17
IO Power		
VCC-PA	Power Supply for GPIO A (1.8V-3.3V)	F20,G20
VCC-PB	Power Supply for GPIO B (1.8V-3.3V)	G19
VCC-PC	Power Supply for GPIO C (1.8V-3.3V)	G7,G8
VCC-PD	Power Supply for GPIO D (1.8V-3.3V)	V21,W21,W22
VCC-PE	Power Supply for GPIO E (1.8V-3.3V)	F18
VCC-PF	Power Supply for GPIO F (1.8V-3.3V)	G6
VCC-PG	Power Supply for GPIO G (1.8V-3.3V)	G18
VCC-PH	Power Supply for GPIO H (1.8V-3.3V)	G15，J14
VCC-PM	Power Supply for GPIO M (1.8V-3.3V)	R19

Signal Name	Description	Ball#
RTC		
VCC_RTC	RTC Power Supply	R21
DRAM Power		
VCC-DRAM	DRAM Power Supply	H7,J7,K7,L7,M6,M7,N6,N7,P6,P7,R7,T7,U7,AA8,AA9,AA10,AA11,AA12,AA13,AA14
VDD-DLL	DLL Power Supply	V9,W9
GND-DRAM	DRAM Ground	T9,T10,U9,U10,V7,V10,W6,W7,W10,Y6,Y7,AA6,AA7,AA15,AA16,AA17,AB14,AB15,AB16,AB17
Audio Codec		
AVCC	Analog Power Supply	L22
AGND	Analog Ground	J19
VRP①	VRP=3.0V, output;	H22
VRA1①	VRA1=1.5V,output;	K22
VRA2①	VRA2=1.5V,output;	J22
VCC-HP	Headphone Power Supply	G21
CPU&GPU		
VDD-CPU	Power Supply for CPU	J15,J16,J17,J18,K15,K16,K17,K18,K19,L15,L16,L17,L18,L19,M15,M16,M17,M18,M19,N15,N16,N17,N18
VDD-GPU	Power Supply for GPU	J9,J10,J11,K9,K10,K11,L9,L10,L11,M9,M10,M11
System		
VDD-SYS	Power Supply for the system	T13,T14,T15,U13,U14,U15,V13,V14,V15,W13,W14,W15
VDD-CPUS	Power Supply for the system	P21，P22
eFUSE		
VDDQE	eFuse Power Supply	P19
Ground		
GND	Ground	F22,J12,J13,K12,K13,K14,L12,L13,L14,M12,M13,M14,N9,N10,N11,N12,N13,N14,P9,P10,P11,P12,P13,P14,P15,P16,P17,P18,R9,R10,R11,R12,R13,R14,R15,R16,R17,R18,T11,T12,T16,T17,T18,U11,U12,U16,U17,U18,U19,V11,V12,V16,W11,W12,Y21,Y22,AA18,AA19,AA20,AA21,AA22,AB18,AB19,AB20,AD24,AE24,AE25

Table 5-4 A31 Power/Ground Signal Description

6 ELECTRICAL CHARACTERISTICS

6.1. ABSOLUTE MAXIMUM RATINGS

Prolonged exposure to absolute maximum ratings (as shown in Table 6-1) may reduce device reliability. Functional operation at these maximum ratings is not implied.

Symbol	Parameter		Min	Max	Unit
$I_{I/O}$	In/Out current for input and output		-40	40	mA
V_{ESD}	ESD stress voltage	HBM(human body mode)	-4K	4K	V_{ESD}
		CDM(charged device mode)	250	250	V
VCC	Power supply for I/O		-0.3	3.6	V
VDD	Power supply for Internal Digital Logic		-0.3	1.4	V
AVCC	Power supply for Analog Part		-0.3	3.6	V
VCC-DRAM	Power supply for DRAM Part		-0.3	1.98	V
VCC-USB	Power supply for USB PHY		-0.3	3.6	V
VCC-LRADC	Power supply for LRADC		-0.3	3.6	V
VCC-HP	Power supply for Headphone		-0.3	3.6	V
VDD-DLL	Power supply for DLL		-0.3	1.4	V
VCC-PLL	Power supply for PLL		-0.3	3.6	V
VDD-CPU	Power Supply for CPU		-0.3	1.4	V
VDD-GPU	Power Supply for GPU		-0.3	1.4	V
T_{STG}	Storage Temperature		-40	125	°C

Table 6-1 Absolute Maximum Ratings

6.2. RECOMMENDED OPERATING CONDITIONS

All A31 modules are used under the operating Conditions contained in Table 6-2.

Symbol	Parameter	Min	Typ	Max	Unit
Ta	Ambient Operating Temperature(Commercial)	-20	/	+70	°C
VCC	Power Supply for the IO	1.7	1.8~3.3	3.6	V
AVCC	Power Supply For Analog Part	2.7	3.0	3.3	V
VCC-DRAM	Power Supply For DRAMC	1.14	1.2~1.8	1.98	V
VCC-USB	Power Supply For USB PHY	2.8	3.3	3.45	V
VCC-LRADC	Power Supply for LRADC	2.7	3.0	3.3	V
VCC-HP	Power Supply For Headphone	3.0	3.3	3.6	V
VDD-DLL	Power Supply For DLL	0.7	1.1	1.32	V
VCC-PLL	Power supply for OSC24M/PLLs	2.7	3.0	3.3	V

VCC-RTC	Power Supply For RTCLDO/LOSC/RCOSC	2.7	3.0	3.3	V
VDD-RTC	Power Supply For RTC/Alarm	0.7	1.1	1.32	V
VDD-SYS	Power supply for VDD_SYS	0.7	1.1	1.32	V
VDD-CPU	Power Supply for CPU	0.7	1.1	1.32	V
VDD-GPU	Power supply for GPU	0.7	1.1	1.32	V

Table 6-2 Recommended Operating Conditions

6.3. DC ELECTRICAL CHARACTERISTICS

Table 6-3 summarizes the DC electrical characteristics of A31.

Symbol	Parameter	Min	Typ	Max	Unit
VIH	High-Level Input Voltage	0.7*VCC	-	VCC+0.3	V
VIL	Low-Level Input Voltage	-0.3	0	0.3*VCC	V
RPU	Input pull-up resistance	50	100	150	KΩ
RPD	Input pull-down resistance	50	100	150	KΩ
IIH	High-Level Input Current	/	10	/	uA
IIL	Low-Level Input Current	/	10	/	uA
VOH	High-Level Output Voltage	VCC-0.2	/	/	V
VOL	Low-Level Output Voltage	/	/	0.2	V
IOZ	Tri-State Output Leakage Current	-10	/	10	uA
CIN	Input Capacitance	/	/	5	pF
COUT	Output Capacitance	/	/	5	pF

Table 6-3 DC Electrical Characteristics

6.4. OSCILLATOR ELECTRICAL CHARACTERISTICS

The A31 clock control module includes 11PLLs, a main oscillator, an on-chip RC oscillator of 466.9KHz ~867.1KHz, and a 32768Hz low power oscillator.

The 24.000MHz frequency is used to generate the main source clock for PLL and the main digital blocks, and the 32768Hz oscillator is used only to provide a low power accurate reference for RTC.

24MHz Oscillator Characteristics

Table 6-4 lists the 24MHz crystal specifications.

Symbol	Parameter	Min	Typ	Max	Unit
$1/(t_{CPMAIN})$	Crystal Oscillator Frequency Range	-	24.000	-	MHz
t_{ST}	Startup Time	–	–		ms
	Frequency Tolerance at 25 °C	-40	–	+40	ppm
	Oscillation Mode	Fundamental			–
	Maximum change over temperature range	-50	–	+50	ppm
P_{ON}	Drive level	–	–	50	uW
C_L	Equivalent Load capacitance	–		–	pF
CL1,CL2	Internal Load capacitance(CL1=CL2)	–		–	pF
R_S	Series Resistance(ESR)	–		–	Ω
	Duty Cycle	30	50	70	%
C_M	Motional capacitance	–	–		pF

C_{SHUT}	Shunt capacitance	–	–		pF
R_{BIAS}	Internal bias resistor				MΩ

Table 6-4 24MHz Oscillator Characteristics

32768Hz Oscillator Characteristics

The 32768Hz crystal is connected between the LOSCI (amplifier input) and LOSCO (amplifier output). Table 6-5 lists the 32768Hz crystal specifications.

Symbol	Parameter	Min	Typ	Max	Unit
$1/(t_{CPMAIN})$	Crystal Oscillator Frequency Range		32.768		kHz
t_{ST}	Startup Time	–	–		ms
	Frequency Tolerance at 25 °C	-40	–	+40	ppm
	Oscillation Mode		Fundamental		–
	Maximum change over temperature range	-50	–	+50	ppm
P_{ON}	Drive level	–	–	50	uW
C_L	Equivalent Load capacitance	–		–	pF
CL1,CL2	Internal Load capacitance(CL1=CL2)	–		–	pF
R_S	Series Resistance(ESR)	–		–	Ω
	Duty Cycle	30	50	70	%
C_M	Motional capacitance	–	–		pF
C_{SHUT}	Shunt capacitance	–	–		pF
R_{BIAS}	Internal bias resistor				MΩ

Table 6-5 32768Hz Oscillator Characteristics

6.5. POWER ON AND POWER OFF SEQUENCE

A31 supports four working modes: active mode, idle mode, super standby mode, and power-off mode.

Power on Sequence

When the system is powered on for the first time, CPU0 will run Boot Rom to scan external storage interface; when the system is powered on from super standby mode, CPU0 will run Boot Rom to check the super standby flag and then jump to internal SRAM.

Following Figure 6-1 illustrates the power on sequence:

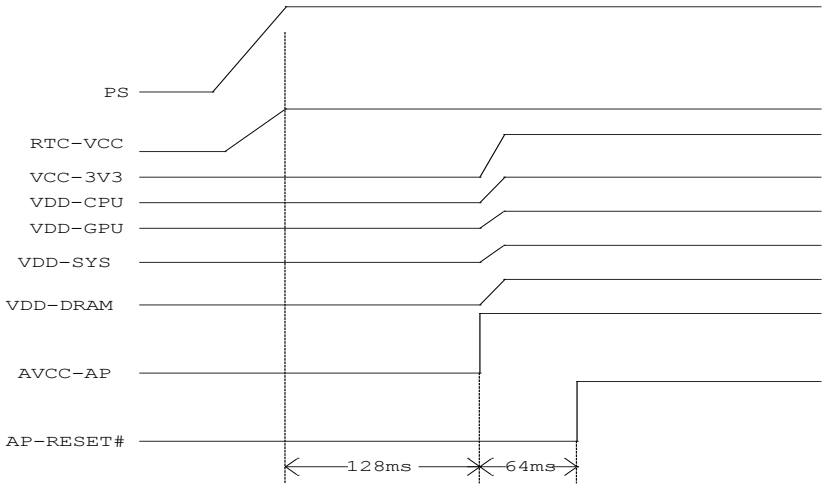


Figure 6-1 A31 Power On Sequence

Power off Sequence

Figure 6-2 illustrates the power off sequence:

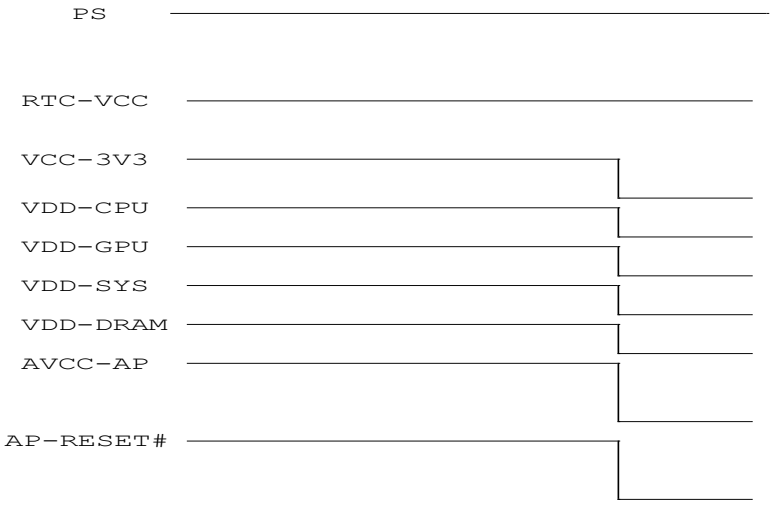


Figure 6-2 A31 Power Off Sequence