A10s Datasheet

V1.40

2012.12.25

Revision History

Version	Date	Author	Description
V1.00	2011.11.30	Allwinner	Initial version
V1.10	2011.12.30		The GPIOE[0]/[1]/[2] and GPIOG[0]/[1]/[2] are changed for INPUT only.
V1.20	2012.03.27		Revise some pin package description.
V1.30	2012.06.18		Revise some pin description.
V1.40	2012.12.25		Correct multiplexing characteristics description

Table of Contents

1. Overview

Allwinner's A10s is a highly cost-effective phablet application solution that combines ARM® Cortex™-A8 CPU together with Mali400 GPU architecture, and thanks to Allwinner's cutting-edge video processing technology, it is also the only phablet solution in current market that is capable of FHD full-format video processing.

To make the total system cost more competitive, A10s features superior system integration, including USB, UART/SPI/TWI, IR, TS controller, TP, I2S/PCM, audio codec, GPS baseband, etc, and also embeds a HDMI controller. Additionally, A10s also supports larger DDR/Nand Flash memory capacity to deliver better system performance and user experience.

2. Features

CPU

- ARM Cortex-A8 Core
- 32KB I-Cache and 32KB D-Cache
- 256KB L2 Cache
- NEON™ SIMD Coprocessor
- Jazelle RCT Acceleration

GPU

3D Graphic Engine

- Support Open GL ES 1.1/ 2.0 and open VG 1.1

VPU

- Video Decoding (FULL HD)
  - Support multi-format video, including VP8, AVS, H.264, H.263, VC-1, MPEG-1/2/4

- Up to 1920*1080@60fps

- Video Encoding
  - Support encoding in H.264 MP format
  - Up to1920*1080@30fps

Display Processing Ability

- Four moveable and size-adjustable layers
- Support multi-format image input
- Support image enhancement processor
- Support Alpha blending / anti-flicker
- Support Hardware cursor
- Support output color correction (luminance / hue / saturation etc)

Display Output Ability

- Support HDMI V1.3/V1.4
- Support CVBS

Image Input Ability

- Camera sensor interface (CSI)

Memory

- 32-bit SDRAM controller

- Support DDR2 SDRAM and DDR3 SDRAM up to 533MHz
- Memory Capacity up to 16 G-bits

- 8-bit NAND Flash Controller with 4 CE and 2RB signals
  - Support SLC/MLC/TLC/DDR NAND
  - 64-bit ECC

External Peripherals

- One USB 2.0 DRD(Dual-Role Device) controller for general application and one USB EHCI/OHCI controller for host application
- Three high-speed memory controllers supporting SD version 3.0 and eMMC version 4.3
- One UART with TX/RX and three UARTs with RTS/CTS
- Three SPI controllers
- Three Two-Wire Interface(TWI) Controllers
- Key Matrix (8x8) with internal debounce filter
- IR controller supporting CIR remoter
- One embedded TS SPI/ SSI for DTV application
- One 10/100Mbps Ethernet MAC
- 2-Ch 6-bit LRADC for line control
- Internal 4-wire touch panel controller with pressure sensor and 2-point touch
- I2S/PCM controller for 2-Ch output
- Internal 24-bit Audio Codec for 2-Ch headphone, 2-Ch microphone, and stereo FM input
- 2-Ch PWM controller

- Embedded GPS baseband

System Peripherals

- 8-Ch normal DMA and 8-Ch dedicated DMA
- Internal 48KB SRAM on chip
- 6 asynchronic timers, 2 synchronic timers, 1 watchdog, and 2 AVS counters

Security System

- Crypto Engine
  - Support DES/3DES/AES encryption and decryption.
  - Support SHA-1, MD5 message digest
  - Support 160-bit hardware PRNG with 192-bit seed
- 128-bit EFUSE chip ID

Package

- TFBGA336package

3. Functional Block Diagram

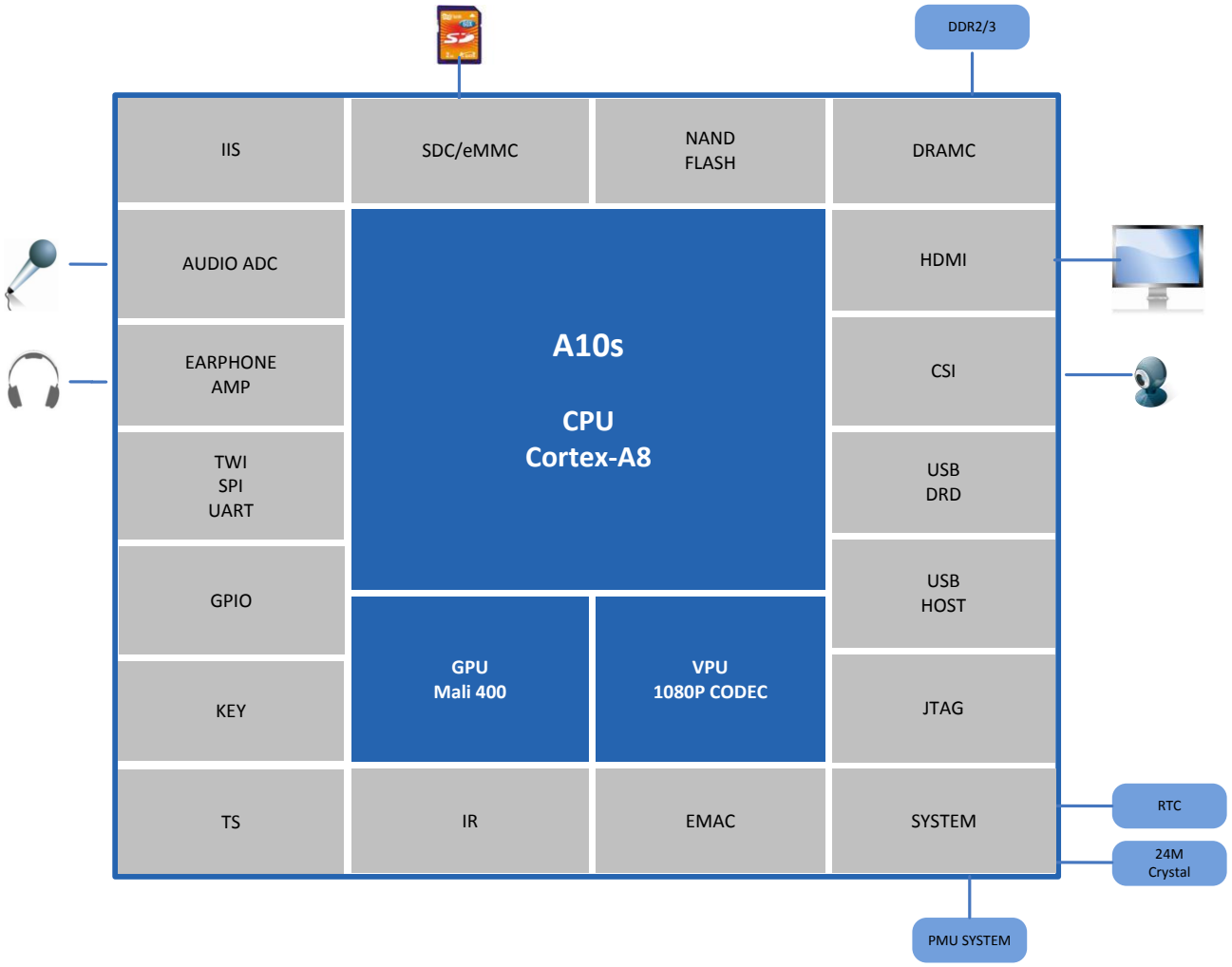
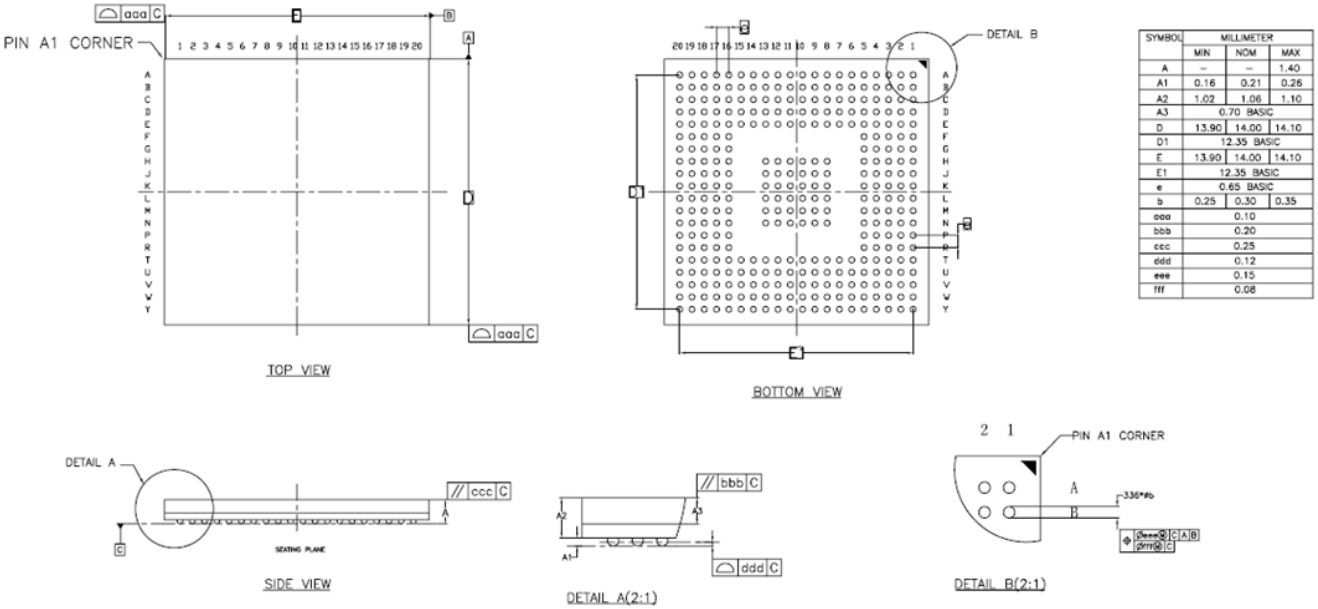


Figure3. A10s Block Diagram

4. Pin Assignments

4.1. Pin Dimension



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	–	–	1.40
A1	0.16	0.21	0.26
A2	1.02	1.06	1.10
A3		0.70 BASIC	
D	13.90	14.00	14.10
D1		12.35 BASIC	
E	13.90	14.00	14.10
E1		12.35 BASIC	
e		0.65 BASIC	
b	0.25	0.30	0.35
aaa		0.10	
bbb		0.20	
ccc		0.25	
ddd		0.12	
eee		0.15	
fff		0.08	

Figure 4-1 A10s Package Dimension

4.2. Pin Map

The following pin maps show the top view of the 336-pin TFBGA package pin assignments.

	1	2	3	4	5	6	7	8	9	10
A	PC6	PC7	PC9	PC12	PC16	PC18	PB17	RESET_N	BOOTS_N	PG1
B	PC5	PC4	PC8	PC11	PC15	PC17	PC19	PB18	NMI_N	PG0
C	PC3	PC2	PC1	PC10	PC14	PA1	PA3	PA5	PA7	PA9
D	PC0	PB5	PB10	TEST	PC13	PA0	PA2	PA4	PA6	PA8
E	PB6	PB7	PB11	PB12	VCC	VDD_CPU	VDD_CPU	VDD_CPU	VDD_CPU	VDD_CPU
F	PB8	PB9	PB13	PB14	VCC					
G	PG9	PG10	PB19	PB20	VDD_EFUSE					
H	PG11	PG12	PG13	VDD_CORE	VDD_CORE			GND	GND	GND
J	SDQ6	SDQ2	SDQ4	V12_DLL	V12_DLL			GND	GND	GND
K	SDQ0	SDQ11	SZQ	GND_DLL	GND_DLL			GND	GND	GND

11	12	13	14	15	16	17	18	19	20	
PG3	PG5	PG7	PB3	PD3	PD7	PD10	PD13	PD14	PD15	A
PG2	PG4	PG6	PG8	PD2	PD6	PD9	PD12	PD16	PD17	B
PA13	PA11	PA15	PA17	PD1	PD5	PD8	PD11	PE11	PE10	C
PA10	PA14	PA12	PA16	PD0	PD4	PD18	PD19	PE9	PE8	D
VDD_CPU	VDD_CPU	VDD_CPU	VDD_CPU	VDD_CORE	VDD_CORE	PD20	PD21	PE7	PE6	E
					VDD_CORE	PD22	PD23	PE5	PE4	F
					VCC	PD24	PD25	PE3	PE2	G
GND	GND	GND			VCC	PD26	PD27	PE1	PE0	H
GND	GND	GND			VCC	PF5	PF4	PB16	PB15	J
GND	GND	GND			VCC	PF3	PF2	PB4	PB2	K

L	SDQ13	SDQ15	SCKE0	SVREF0	GND_DRAM			GND	GND	GND
M	SDQ9	SDQM1	SA10	SODT1	VCC_DRAM			GND	GND	GND
N	SDQS0	SDQS0_N	SBA1	SCS1	VCC_DRAM			GND	GND	GND
P	SDQM0	SDQS1	SA4	SA12	GND_DRAM					
R	SDQS1_N	SDQ12	SA6	SA1	GND_DRAM					
T	SDQ8	SDQ14	SA8	SA11	VCC_DRAM	VCC_DRAM	GND_DRAM	GND_DRAM	VCC_DRAM	VCC_DRAM
U	SDQ10	SDQ1	SA14	SRAS	CKE1	SBA0	SA3	SA2	SA13	SRST
V	SDQ3	SDQ7	SWE	SCAS	SCS0	SBA2	SA0	SA5	SA9	SA7
W	SDQ5	SCK	SDQ22	SDQ16	SDQ29	SDQ25	SDQS2	SDQM2	SDQS3	SDQ28
Y	SCK_N	SDQ20	SDQ18	SDQ27	SDQ31	SDQM3	SDQS2_N	SDQ24	SDQS3_N	SDQ26
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**

GND	GND	GND			VCC	PF1	PF0	PB1	PB0	L
GND	GND	GND			VDD_CORE	VDD_CORE	TVOUT	JTAG1_N	JTAG0_N	M
GND	GND	GND			GND_USB	UDP1	UDM1	HTX2N	HTX2P	N
					V33_USB	UDP0	UDM0	HTX1N	HTX1P	P
					V33_HDMI	HCEC	HSCL	HTX0N	HTX0P	R
VCC_DRAM	GND_DRAM	VDD_CORE	V33_HP	AVCC	V33_PLL	HHPD	HSDA	HTXCN	HTXCP	T
SVREF1	GND_DRAM	VDD_CORE	HPBP	GND_HP	AGND	LINEINL	HVREG1	HVREG2	X24MIN	U
SODT0	SDQ19	HPCOMFB	VRA2	VRA1	FMINR	PLLTEST	LINEINR	GND	X24MOUT	V
SDQ30	SDQ21	HPCOM	VRP	MICIN2	FMINL	MIC1OUTP	MIC1OUTN	TPY2	TPY1	W
SDQ17	SDQ23	HPL	HPR	MICIN1	VMIC	LRADC0	LRADC1	TPX2	TPX1	Y
11	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	

Figure 4-2 TFBGA336 Pin Map-Top View

5. Pin Description

5.1. Pin Characteristics

1. **BALL#:** Ball numbers on the bottom side associated with each signals on the bottom.
2. **Pin Name:** Names of signals multiplexed on each ball (also notice that the name of the pin is the signal name in function 0).
3. **Function:** Multiplexing function number.

   Function 0 is the the default function, but is not necessarily the primary mode.

   Functions 1 to 7 are possible modes for alternate functions.
4. **Type:** signal direction
   - I = Input
   - O = Output
   - I/O = Input/Output
   - A = Analog
   - AIO = Analog Input/Output
   - PWR = Power
   - GND = Ground
5. **Pin Reset State:** The state of the terminal at reset (power up).
   - 0: The buffer drives VOL(pull down/pull up resistor not activated)
   - 0 (PD): The buffer drives V_{OL} with an active pull down resistor.
   - 1: The buffer drives VOH (pull down/pull up resistor not activated).
   - 1 (PU): The buffer drives V_{OH} with an active pull up resistor.
   - Z: High-impedance
   - L: High-impedance with an active pull down resistor.
   - H: High-impedance with an active pull up resistor.
6. **Pull Up/Down:** Denotes the presence of an internal pull up or pull down resister. Pull up and pull down resistor can be enabled or disabled via software.
7. **Buffer Strength:** Drive strength of the associated output buffer.

Ball	Pin Name	Type	Reset State	Pull Up/Down	Buffer Strength
K1	SDQ0	I/O			
	DDR2_D6				
	DDR3_D0				
U2	SDQ1	I/O			
	DDR2_D7				
	DDR3_D1				
J2	SDQ2	I/O			
	DDR2_D1				
	DDR3_D2				
V1	SDQ3	I/O			
	DDR2_D0				
	DDR3_D3				
J3	SDQ4	I/O			
	DDR2_D4				
	DDR3_D4				
W1	SDQ5	I/O			
	DDR2_D5				
	DDR3_D5				
J1	SDQ6	I/O			
	DDR2_D3				
	DDR3_D6				
V2	SDQ7	I/O			
	DDR2_D2				
	DDR3_D7				
T1	SDQ8	I/O			
	DDR2_D8				
	DDR3_D8				

M1	SDQ9	I/O			
	DDR2_D11				
	DDR3_D9				
U1	SDQ10	I/O			
	DDR2_D13				
	DDR3_D10				
K2	SDQ11	I/O			
	DDR2_D12				
	DDR3_D11				
R2	SDQ12	I/O			
	DDR2_D15				
	DDR3_D12				
L1	SDQ13	I/O			
	DDR2_D9				
	DDR3_D13				
T2	SDQ14	I/O			
	DDR2_D10				
	DDR3_D14				
L2	SDQ15	I/O			
	DDR2_D14				
	DDR3_D15				
W4	SDQ16	I/O			
	DDR2_D22				
Y11	SDQ17	I/O			
	DDR2_D23				
Y3	SDQ18	I/O			
	DDR2_D17				
V12	SDQ19	I/O			

	DDR2_D16				
Y2	SDQ20	I/O			
	DDR2_D20				
W12	SDQ21	I/O			
	DDR2_D21				
W2	SDQ22	I/O			
	DDR2_D19				
Y12	SDQ23	I/O			
	DDR2_D18				
Y8	SDQ24	I/O			
	DDR2_D24				
W6	SDQ25	I/O			
	DDR2_D27				
Y10	SDQ26	I/O			
	DDR2_D29				
Y4	SDQ27	I/O			
	DDR2_D28				
W10	SDQ28	I/O			
	DDR2_D31				
W5	SDQ29	I/O			
	DDR2_D25				
W11	SDQ30	I/O			
	DDR2_D26				
Y5	SDQ31	I/O			
	DDR2_D30				
N1	SDQS0	I/O			
	DDR2_DQS0				
	DDR3_DQS0				

P2	SDQS1	I/O			
	DDR2_DQS1				
	DDR3_DQS1				
W7	SDQS2	I/O			
	DDR2_DQS2				
W9	SDQS3	I/O			
	DDR2_DQS3				
N2	SDQS0#	I/O			
	DDR2_DQS0#				
	DDR3_DQS0#				
R1	SDQS1#	I/O			
	DDR2_DQS1#				
	DDR3_DQS1#				
Y7	SDQS2#	I/O			
	DDR2_DQS2#				
Y9	SDQS3#	I/O			
	DDR2_DQS3#				
V7	SA0	O			
	DDR2_BA1				
R4	SA1	O			
	DDR2_A2				
U8	SA2	O			
	DDR2_A1				
U7	SA3	O			
	DDR2_BA0				
P3	SA4	O			
	DDR2_A0				
V8	SA5	O			

	DDR2_A10				
R3	SA6	O			
	DDR2_A4				
V10	SA7	O			
	DDR2_A7				
T3	SA8	O			
	DDR2_A6				
V9	SA9	O			
	DDR2_A3				
M3	SA10	O			
	DDR2_RAS				
	DDR3_A10				
T4	SA11	O			
	DDR2_A8				
P4	SA12	O			
	DDR2_CAS				
	DDR3_A12				
U9	SA13	O			
	DDR2_A5				
U3	SA14	O			
	DDR2_A14				
P1	SDQM0	O			
	DDR2_DM0				
	DDR3_DM0				
M2	SDQM1	O			
	DDR2_DM1				
	DDR3_DM1				
W8	SDQM2	O			

	DDR2_DM2				
Y6	SDQM3	O			
	DDR2_DM3				
W2	SCK	O			
	DDR2_CK				
	DDR3_CK				
Y1	SCK#	O			
	DDR2_CK#				
	DDR3_CK#				
L3	SCKE0	O			
	DDR2_ODT0				
	DDR3_CKE0				
U5	SCKE1	O			
	DDR2_CKE1				
U6	SBA0	O			
	DDR2_BA2				
N3	SBA1	O			
	DDR2_CS0				
	DDR3_BA1				
V6	SBA2	O			
	DDR2_WE				
V5	SCS0	O			
	DDR3_CS0				
N4	SCS1	O			
	DDR2_CS1				
	DDR3_CS1				
V11	SODT0	O			
	DDR2_A12				

M4	SODT1	O			
	DDR2_ODT1				
	DDR3_ODT1				
U4	SRAS	O			
	DDR2_A11				
V4	SCAS	O			
	DDR2_A13				
V3	SWE	O			
	DDR2_CKE0				
U10	SRST	O			
	DDR2_A9				
K3	SZQ	A			
L4	SVREF0	P			
U11	SVREF1	P			
J4/J5	VDD_DLL	P			
K4/K5	GND_DLL	G			
D6	PA0	I/O			
	ERXD3				
	TS_CLK				
	KP_IN0				
C6	PA1	I/O			
	ERXD2				
	TS_ERR				
	KP_IN1				
D7	PA2	I/O			
	ERXD1				
	TS_SYNC				
	KP_IN2				

C7	PA3	I/O			
	ERXD0				
	TS_DVLD				
	KP_IN3				
D8	PA4	I/O			
	ETXD3				
	TS_DO				
	KP_IN4				
C8	PA5	I/O			
	ETXD2				
	TS_D1				
	KP_IN5				
D9	PA6	I/O			
	ETXD1				
	TS_D2				
	KP_IN6				
C9	PA7	I/O			
	ETXD0				
	TS_D3				
	KP_IN7				
D10	PA8	I/O			
	ERXCK				
	TS_D4				
	KP_OUT0				
C10	PA9	I/O			
	ERXERR				
	TS_D5				
	KP_OUT1				

D11	PA10	I/O			
	ERXDV				
	TS_D6				
	KP_OUT2				
C12	PA11	I/O			
	EMDC				
	TS_D7				
	KP_OUT3				
D13	PA12	I/O			
	EMDIO				
	UART1_TX				
	KP_OUT4				
C11	PA13	I/O			
	ETXEN				
	UART1_RX				
	KP_OUT5				
D12	PA14	I/O			
	ETXCK				
	UART1_CTS				
	UART3_TX				
	KP_OUT6				
C13	PA15	I/O			
	ECRS				
	UART1_RTS				
	UART3_RX				
	KP_OUT7				
D14	PA16	I/O			
	ECOL				

	UART2_TX				
C14	PA17	I/O			
	ETXERR				
	UART2_RX				
	EINT31				
L20	PB0	I/O			
	TWI0_SCK				
L19	PB1	I/O			
	TWI0_SDA				
K20	PB2	I/O			
	PWM0				
	/				
	EINT16				
A14	PB3	I/O			
	IR_TX				
	EINT17				
K19	PB4	I/O			
	IR_RX				
	EINT18				
D2	PB5	I/O			
	I2S_MCLK				
	EINT19				
E1	PB6	I/O			
	I2S_BCLK				
	EINT20				
E2	PB7	I/O			
	I2S_LRCK				
	EINT21				

F1	PB8	I/O			
	I2S_DO				
	EINT22				
F2	PB9	I/O			
	I2S_DI				
	/				
	EINT23				
D3	PB10	I/O			
	SPI2_CS1				
	/				
	EINT24				
E3	PB11	I/O			
	SPI2_CS0				
	JTAG_MS0				
	EINT25				
E4	PB12	I/O			
	SPI2_CLK				
	JTAG_CK0				
	EINT26				
F3	PB13	I/O			
	SPI2_MOSI				
	JTAG_DO0				
	EINT27				
F4	PB14	I/O			
	SPI2_MISO				
	JTAG_DI0				
	EINT28				
J20	PB15	I/O			

	TWI1_SCK				
J19	PB16	I/O			
	TWI1_SDA				
A7	PB17	I/O			
	TWI2_SCK				
B8	PB18	I/O			
	TWI2_SDA				
G3	PB19	I/O			
	UART0_TX				
	EINT29				
G4	PB20	I/O			
	UART0_RX				
	EINT30				
D1	PC0	I/O			
	NWE				
	SPI0_MOSI				
C3	PC1	I/O			
	NALE				
	SPI0_MISO				
C2	PC2	I/O			
	NCLE				
	SPI0_CLK				
C1	PC3	I/O		Pull-up	
	NCE1				
	SPI0_CS0				
B2	PC4	I/O		Pull-up	
	NCE0				
B1	PC5	I/O			

	NRE				
A1	PC6	I/O		Pull-up	
	NRB0				
	SDC2_CMD				
A2	PC7	I/O		Pull-up	
	NRB1				
	SDC2_CLK				
B3	PC8	I/O			
	NDQ0				
	SDC2_D0				
A3	PC9	I/O			
	NDQ1				
	SDC2_D1				
C4	PC10	I/O			
	NDQ2				
	SDC2_D2				
B4	PC11	I/O			
	NDQ3				
	SDC2_D3				
A4	PC12	I/O			
	NDQ4				
	SDC2_D4				
D5	PC13	I/O			
	NDQ5				
	SDC2_D5				
C5	PC14	I/O			
	NDQ6				
	SDC2_D6				

B5	PC15	I/O			
	NDQ7				
	SDC2_D7				
A5	PC16	I/O		Pull-down	
	NWP				
	UART3_TX				
B6	PC17	I/O		Pull-up	
	NCE2				
	UART3_RX				
A6	PC18	I/O		Pull-up	
	NCE3				
	UART2_TX				
	UART3_CTS				
B7	PC19	I/O			
	NDQS				
	UART2_RX				
	UART3_RTS				
D15	PD0	I/O			
C15	PD1	I/O			
B15	PD2	I/O			
	UART2_TX				
A15	PD3	I/O			
	UART2_RX				
D16	PD4	I/O			
	UART2_CTS				
C16	PD5	I/O			
	UART2_RTS				
B16	PD6	I/O			

	ECRS				
A16	PD7	I/O			
	ECOL				
C17	PD8	I/O			
B17	PD9	I/O			
A17	PD10	I/O			
	ERXDO				
C18	PD11	I/O			
	ERXD1				
B18	PD12	I/O			
	ERXD2				
A18	PD13	I/O			
	ERXD3				
A19	PD14	I/O			
	ERXCK				
A20	PD15	I/O			
	ERXERR				
B19	PD16	I/O			
B20	PD17	I/O			
D17	PD18	I/O			
	ERXDV				
D18	PD19	I/O			
	ETXD0				
E17	PD20	I/O			
	ETXD1				
E18	PD21	I/O			
	ETXD2				
F17	PD22	I/O			

	ETXD3				
F18	PD23	I/O			
	ETXEN				
G17	PD24	I/O			
	ETXCK				
G18	PD25	I/O			
	ETXERR				
H17	PD26	I/O			
	EMDC				
H18	PD27	I/O			
	EMDIO				
H20	PE0	I/O			
	TS_CLK				
	CSI_PCLK				
	SPI2_CS0				
H19	PE1	I/O			
	TS_ERR				
	CSI_MCLK				
	SPI2_CLK				
G20	PE2	I/O			
	TS_SYNC				
	CSI_HSYNC				
	SPI2_MOSI				
G19	PE3	I/O			
	TS_DVLD				
	CSI_VSYNC				
	SPI2_MISO				
F20	PE4	I/O			

	TS_D0				
	CSI_D0				
	SDC2_DO				
F19	PE5	I/O			
	TS_D1				
	CSI_D1				
	SDC2_D1				
E20	PE6	I/O			
	TS_D2				
	CSI_D2				
	SDC2_D2				
E19	PE7	I/O			
	TS_D3				
	CSI_D3				
	SDC2_D3				
D20	PE8	I/O			
	TS_D4				
	CSI_D4				
	SDC2_CMD				
D19	PE9	I/O			
	TS_D5				
	CSI_D5				
	SDC2_CLK				
C20	PE10	I/O			
	TS_D6				
	CSI_D6				
	UART_TX				
C19	PE11	I/O			

	TS_D7				
	CSI_D7				
	UART_RX				
L18	PF0	I/O			
	SDC0_D1				
	JTAG_MS1				
L17	PF1	I/O			
	SDC0_D0				
	JTAG_DI1				
K18	PF2	I/O			
	SDC0_CLK				
	UART0_TX				
K17	PF3	I/O			
	SDC0_CMD				
	JTAG_DO1				
J18	PF4	I/O			
	SDC0_D3				
	UART0_RX				
J17	PF5	I/O			
	SDC0_D2				
	JTAG_CK1				
B10	PG0	I/O			
	GPS_CLK				
	EINT0				
A10	PG1	I/O			
	GPS_SIGN				
	EINT1				
B11	PG2	I/O			

	GPS_MAG				
	EINT2				
A11	PG3	I/O			
	SDC1_CMD				
	/				
	UART1_TX				
	EINT3				
B12	PG4	I/O			
	SDC1_CLK				
	/				
	UART1_RX				
	EINT4				
A12	PG5	I/O			
	SDC1_D0				
	/				
	UART1_CTS				
	EINT5				
B13	PG6	I/O			
	SDC1_D1				
	/				
	UART1_RTS				
	UART2_RTS				
	EINT6				
A13	PG7	I/O			
	SDC1_D2				
	/				
	UART2_TX				
	EINT7				

B14	PG8	I/O			
	SDC1_D3				
	/				
	UART2_RX				
	EINT8				
G1	PG9	I/O			
	SPI1_CS0				
	UART3_TX				
	EINT9				
G2	PG10	I/O			
	SPI1_CLK				
	UART3_RX				
	EINT10				
H1	PG11	I/O			
	SPI1_MOSI				
	UART3_CTS				
	EINT11				
H2	PG12	I/O			
	SPI1_MISO				
	UART3_RTS				
	EINT12				
H3	PG13	I/O			
	SPI1_CS1				
	PWM1				
	UART2_CTS				
	EINT13				
G5	VDD-EFUSE	P			
A9	UBOOT			Pull_up	

M20	JTAG_SEL0			Pull_up	
M19	JTAG_SEL1			Pull_up	
D4	TEST			Pull_down	
B9	NMI#			No-pull	
A8	RESET#				
T17	HHPD				
T18	HSDA				
R18	HSCL				
R17	HCEC				
U18	HVREG1				
U19	HVREG2				
T20	HTXCP				
T19	HTXCN				
R20	HTX0P				
R19	HTX0N				
P20	HTX1P				
P19	HTX1N				
N20	HTX2P				
N19	HTX2N				
R16	V33_HDMI				
M18	TVOUT				
P18	DM0				
P17	DP0				
N18	DM1				
N17	DP1				
P16	V33_USB				
N16	GND_USB				
Y20	X1				

Y19	X2				
W20	Y1				
W19	Y2				
W16	FMINL				
V16	FMINR				
W17	MIC1OUTP				
VW18	MIC1OUTN				
Y16	VMIC				
W15	MINCIN2				
Y15	MINCIN1				
V15	VRA1				
V14	VRA2				
T15	AVCC				
W14	VRP				
U16	AGND				
Y14	HPOUTR				
U15	GND_HP				
W13	HPCOM				
V13	HPCOMFB				
T14	V33_HP				
U14	HPBP				
Y13	HPOUTL				
Y17	LRADC0				
Y18	LRADC1				
U20	X24MIN				
V20	X24MOUT				
V17	PLLTEST				
U17	LINEINL				

V18	LINEINR				
T16	V33_PLL				
E5/F5/G16/H16/J16/K16/L16	VCC(7)				
M5/N5/T5/T6/T9/T10/T11	VCC_DRAM(7)				
L5/P5/R5/T7/T8/T12/U12	GND_DRAM(7)				
E6/E7/E8/E9/E10/E11/E12/E13/E14	VDD_CPU(9)				
E15/E16/F16/H4/H5/T13/U13/M16/M17	VDD_CORE(9)				
V19/H8/H9/H10/H11/H12/H13/J8/J9/J10/J11/J12/J13/K8/K9/K10/K11/K12/K13/L8/L9/L10/L11/L12/L13/M8/M9/M10/M11/M12/M13/N8/N9/N10/N11/N12/N13	GND(37)				

Table 5-1 Pin Characteristics

5.2. Multiplexing Characteristics

The following tables provide a description of the A10s multiplexing on the TFBGA336 package.

Note: The PE0/PE1/PE2 / PG0/PG1/PG2 are for input only.

Port	Multiplex Function Select

	Default	Multi2	Multi3	Multi4	Multi5	Multi6
PA0	PA0	ERXD3	TS_CLK		KP_IN0	
PA1	PA1	ERXD2	TS_ERR		KP_IN1	
PA2	PA2	ERXD1	TS_SYNC		KP_IN2	
PA3	PA3	ERXD0	TS_DVLD		KP_IN3	
PA4	PA4	ETXD3	TS_D0		KP_IN4	
PA5	PA5	ETXD2	TS_D1		KP_IN5	
PA6	PA6	ETXD1	TS_D2		KP_IN6	
PA7	PA7	ETXD0	TS_D3		KP_IN7	
PA8	PA8	ERXCK	TS_D4	UART1_DTR	KP_OUT0	
PA9	PA9	ERXERR	TS_D5	UART1_DSR	KP_OUT1	
PA10	PA10	ERXDV	TS_D6	UART1_DCD	KP_OUT2	
PA11	PA11	EMDC	TS_D7	UART1_RING	KP_OUT3	
PA12	PA12	EMDIO	UART1_TX		KP_OUT4	
PA13	PA13	ETXEN	UART1_RX		KP_OUT5	
PA14	PA14	ETXCK	UART1_CTS	UART3_TX	KP_OUT6	
PA15	PA15	ECRS	UART1_RTS	UART3_RX	KP_OUT7	
PA16	PA16	ECOL	UART2_TX			
PA17	PA17	ETXERR	URAT2_RX			EINT31
PB0	PB0	TWI0_SCK				
PB1	PB1	TWI0_SDA				
PB2	PB2	PWM0				EINT16
PB3	PB3	IR_TX				EINT17
PB4	PB4	IR_RX				EINT18
PB5	PB5	I2S_MCLK				EINT19
PB6	PB6	I2S_BCLK				EINT20
PB7	PB7	I2S_LRCK				EINT21
PB8	PB8	I2S_DO				EINT22

PB9	PB9	I2S_DI				EINT23
PB10	PB10	SPI2_CS1				EINT24
PB11	PB11	SPI2_CS0	JTAG_MS0			EINT25
PB12	PB12	SPI2_CLK	JTAG_CK0			EINT26
PB13	PB13	SPI2_MOSI	JTAG_DO0			EINT27
PB14	PB14	SPI2_MISO	JTAG_DI0			EINT28
PB15	PB15	TWI1_SCK				
PB16	PB16	TWI1_SDA				
PB17	PB17	TWI2_SCK				
PB18	PB18	TWI2_SDA				
PB19	PB19	UART0_TX				EINT29
PB20	PB20	UART0_RX				EINT30
PC0	PC0	NWE	SPI0_MOSI			
PC1	PC1	NALE	SPI0_MISO			
PC2	PC2	NCLE	SPI0_CLK			
PC3	PC3	NCE1	SPI0_CS0			
PC4	PC4	NCE0				
PC5	PC5	NRE				
PC6	PC6	NRB0	SDC2_CMD			
PC7	PC7	NRB1	SDC2_CLK			
PC8	PC8	NDQ0	SDC2_D0			
PC9	PC9	NDQ1	SDC2_D1			
PC10	PC10	NDQ2	SDC2_D2			
PC11	PC11	NDQ3	SDC2_D3			
PC12	PC12	NDQ4	SDC2_D4			
PC13	PC13	NDQ5	SDC2_D5			
PC14	PC14	NDQ6	SDC2_D6			
PC15	PC15	NDQ7	SDC2_D7			

PC16	PC16	NWP		UART3_TX		
PC17	PC17	NCE2		UART3_RX		
PC18	PC18	NCE3	UART2_TX	UART3_CTS		
PC19	PC19	NDQS	URAT2_RX	UART3_RTS		
PD0	PD0					
PD1	PD1					
PD2	PD2	UART2_TX				
PD3	PD3	UART2_RX				
PD4	PD4	UART2_CTS				
PD5	PD5	UART2_RTS				
PD6	PD6	ECRS				
PD7	PD7	ECOL				
PD8	PD8					
PD9	PD9					
PD10	PD10	ERXD0				
PD11	PD11	ERXD1				
PD12	PD12	ERXD2				
PD13	PD13	ERXD3				
PD14	PD14	ERXCK				
PD15	PD15	ERXERR				
PD16	PD16					
PD17	PD17					
PD18	PD18	ERXDV				
PD19	PD19	ETXD0				
PD20	PD20	ETXD1				
PD21	PD21	ETXD2				
PD22	PD22	ETXD3				
PD23	PD23	ETXEN				

PD24	PD24	ETXCK				
PD25	PD25	ETXERR				
PD26	PD26	EMDC				
PD27	PD27	EMDIO				
PE0	PE0	TS_CLK	CSI_PCLK	SPI2_CS0		EINT14
PE1	PE1	TS_ERR	CSI_MCLK	SPI2_CLK		EINT15
PE2	PE2	TS_SYNC	CSI_HSYNC	SPI2_MOSI		
PE3	PE3	TS_DVLD	CSI_VSYNC	SPI2_MISO		
PE4	PE4	TS_D0	CSI_D0	SDC2_D0		
PE5	PE5	TS_D1	CSI_D1	SDC2_D1		
PE6	PE6	TS_D2	CSI_D2	SDC2_D2		
PE7	PE7	TS_D3	CSI_D3	SDC2_D3		
PE8	PE8	TS_D4	CSI_D4	SDC2_CMD		
PE9	PE9	TS_D5	CSI_D5	SDC2_CLK		
PE10	PE10	TS_D6	CSI_D6	UART1_TX		
PE11	PE11	TS_D7	CSI_D7	UART1_RX		
PF0	PF0	SDC0_D1		JTAG_MS1		
PF1	PF1	SDC0_D0		JTAG_DI1		
PF2	PF2	SDC0_CLK		UART0_TX		
PF3	PF3	SDC0_CMD		JTAG_DO1		
PF4	PF4	SDC0_D3		UART0_RX		
PF5	PF5	SDC0_D2		JTAG_CK1		
PG0	PG0	GPS_CLK				EINT0
PG1	PG1	GPS_SIGN				EINT1
PG2	PG2	GPS_MAG				EINT2
PG3	PG3	SDC1_CMD	/	UART1_TX		EINT3
PG4	PG4	SDC1_CLK	/	UART1_RX		EINT4
PG5	PG5	SDC1_D0	/	UART1_CTS		EINT5

PG6	PG6	SDC1_D1	/	UART1_RTS	UART2_RTS	EINT6
PG7	PG7	SDC1_D2	/		UART2_TX	EINT7
PG8	PG8	SDC1_D3	/		URAT2_RX	EINT8
PG9	PG9	SPI1_CS0	UART3_TX			EINT9
PG10	PG10	SPI1_CLK	UART3_RX			EINT10
PG11	PG11	SPI1_MOSI	UART3_CTS			EINT11
PG12	PG12	SPI1_MISO	UART3_RTS			EINT12
PG13	PG13	SPI1_CS1	PWM1		UART2_CTS	EINT13

Table5-2 Pin Multiplex Function Select Table

5.3. Power and Miscellaneous Signals

Many signals are available on multiple pins according to the software configuration of the multiplexing options.

1. Signal Name: The signal name
2. Description: Description of the signal
3. Type: Pin type for this specific function:
   - I = Input
   - O = Output
   - Z = High-impedance
   - A = Analog
   - PWR = Power
   - GND = Ground
4. Pin #: Associated ball(s) number

5.3.1. Power Domain Signal Description

Signal Name	Description	Pin Name	Ball#
HDMI			
V33_HDMI	HDMI Power Supply	V33_HDMI	R16

Signal Name	Description	Pin Name	Ball#
Audio DAC Power			
GND_HP	Headphone Ground	GND_HP	U15
V33_HP	Headphone Power Supply	V33_HP	T14
Audio ADC Power			
VMIC	Microphone ADC Power Supply	VMIC	Y16
USB Power			
V33_USB	USB Power Supply	V33_USB	P16
GND33_USB	USB Ground	GND33_USB	N16
PLL Power			
V33_PLL	PLL Power Supply	V33_PLL	T16
Core Power			
VDD	Core Chip Power Supply	VDD(9)	E15/E16/F16/H4/H5/T13/U13/M16/M17
GND	Core Chip Ground	GND(37)	V19/H8/H9/H10/H11/H12/H13/J8/J9/J10/J11/J12/J13/K8/K9/K10/K11/K12/K13/L8/L9/L10/L11/L12/L13/M8/M9/M10/M11/M12/M13/N8/N9/N10/N11/N12/N13
IO Power			
VCC	IO Power Supply	VCC(7)	E5/F5/G16/H16/J16/K16/L16
CPU Power			
VDD_CPU	CPU Power Supply	VDD_CPU(9)	E6/E7/E8/E9/E10/E11/E12/E13/E14
DRAM Power			

Signal Name	Description	Pin Name	Ball#
VCC_ DRAM	DRAM Power Supply	VCC_ DRAM (7)	M5/N5/T5/T6/T9/T10/T11
GND_DRAM	DRAM Ground	GND_DRAM (7)	L5/P5/R5/T7/T8/T12/U12
SDRAM Power			
V12_DLL	SDRAM Power Supply	V12_DLL (2)	J4/J5
GND_DLL	SDRAM Ground	GND_DLL(2)	K4/K5
Analog Power			
AVCC	Analog Power Supply	AVCC	T15
AGND	Analog Ground	AGND	U16

Table 5-3 Power Domain Signal Description

5.3.2. Miscellaneous Signal Description

Signal Name	Description	Type	Pin Name	Ball#
JTAG Interface				
JTAG_SEL0	JTAG port Select bit0	I	JTAG_SEL0	M20
JTAG_SEL1	JTAG Port Select Bit1	I	JTAG_SEL1	M19
JTAG Port 0				
JTAG_MS0	JTAG Mode Select	I	PB11	E3
JTAG_CK0	JTAG Clock	I	PB12	E4
JTAG_DO0	JTAG test DataOutput	O	PB13	F3
JTAG_DI0	JTAG test Data Input	I	PB14	F4
JTAG Port 1				
JTAG_MS1	JTAG Mode Select	I/O	PF0	L18
JTAG_CK1	JTAG Clock	I/O	PF5	J17
JTAG_DO1	JTAG test DataOutput	I/O	PF3	K17

Signal Name	Description	Type	Pin Name	Ball#
JTAG_DI1	JTAG test Data Input	I/O	PF1	L17
Clock				
X24MIN	Main 24MHz crystal Input for internal OSC	I	X24MIN	U20
X24MOUT	Main 24MHz crystal Output for internal OSC	O	X24MOUT	V20
Reset				
RESET#	System Reset	I	RESET#	A8
FIQ				
NMI#	External Fast Interrupt Request	I	NMI#	B9
Boot				
UBOOT	Boot Mode	I	UBOOT	A9
Test				
TEST	Test Pin (Pull down Internal default)	I	TEST	D4
Others				
VRP	Internal Reference Voltage	A	VRP	W14
VRA1	Internal Reference Voltage	A	VRA1	V15
VRA2	Internal Reference Voltage	A	VRA2	V14

Table 5-4 Miscellaneous Signal Description

6. Electrical Characteristics

6.1. Absolute Maximum Ratings

The absolute maximum ratings (shown in Table 6-1) define limitations for electrical and thermal stresses. These limits prevent permanent damage to the A10s.

Note: Absolute maximum ratings are not operating ranges. Operation at absolute maximum ratings is not guaranteed.

Symbol	Parameter		MIN	MAX	Unit
TS	Storage Temperature		-40	125	℃
II/O	In/Out current for input and output		-40	40	mA
VESD	ESD stress voltage	HBM(human body model)	-4K	4K	VESD
		CDM(charged device model)	250	250	V
VCC	DC Supply Voltage for I/O		-0.3	3.6	V
VDD	DC Supply Voltage for Internal Digital Logic		-0.3	1.32	V
VCC_ANALOG	DC Supply Voltage for Analog Part		-0.3	3.6	V
VCC_DRAM	DC Supply Voltage for DRAM Part		-0.3	1.98	V
VCC_USB	DC Supply Voltage for USB PHY		-0.3	3.6	V
VCC_TV	DC Supply Voltage for TV-OUT DAC		-0.3	3.6	V
VCC_LRADC	DC Supply Voltage for LRADC		-0.3	3.0	V
VCC_HP	DC Supply Voltage for Headphone		-0.3	3.6	V
VDD_PLL	DC Supply Voltage for PLL		-0.3	1.32	V

Table 6-1 Multiplexing Characteristics

6.2. Recommended Operating Conditions

All A10s modules are used under the operating Conditions contained in Table 6-2.

Symbol	Parameter	Min	Typ	Max	Unit
Ta	Operating Temperature[Commercial]	-20	–	+70	℃
VCC	DC Supply Voltage for I/O	1.7	1.8~3.3	3.6	V
VDD	DC Supply Voltage for Internal Digital Logic	1.1	1.2	1.3	V
VCC_ANALOG	DC Supply Voltage for Analog Part	2.7	3.0	3.3	V
VCC_DRAM	DC Supply Voltage for DRAM Part	1.425	1.5~1.8	1.98	V
VCC_USB	DC Supply Voltage for USB PHY	3.0	3.3	3.45	V
VCC_TV	DC Supply Voltage for TV-OUT DAC	3.0	3.3	3.6	V

Table 6-2 Recommended Operating Conditions

6.3. DC Electrical Characteristics

Table 6-3 summarizes the DC electrical characteristics of A10s.

Symbol	Parameter	Min	Typ	Max	Unit
VIH	High-level input voltage	0.7*VCC	-	VCC+0.3	V
VIL	Low-level input voltage	-0.3	-	0.3*VCC	V
IIH	High-level input current	-	-	10	uA
IIL	Low-level input current	-	-	10	uA
VOH	High-level output voltage	VCC-0.2	-	VCC	V
VOL	Low-level output voltage	0	-	0.2	V
IOZ	Tri-State Output Leakage Current	-10	-	10	uA
CIN	Input capacitance	-	-	5	pF
COUT	Output capacitance	-	-	5	pF

Table 6-3 DC Electrical Characteristics

6.4. Oscillator Electrical Characteristics

The A10s contains a 24.000 MHz oscillator.The A10s device operation requires the following input clock:

- The 24.000MHz frequency is used to generate the main source clock of the A10s device.

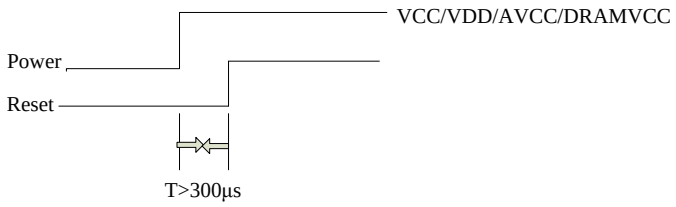
6.4.1. 24MHz Oscillator Characteristics

Table 6-4 lists the 24MHz crystal specifications.

Symbol	Parameter	Min	Typ	Max	Unit
1/(tCPMAIN)	Crystal Oscillator Frequency Range		24.000		MHz
tST	Startup Time	–	–		ms
	Frequency Tolerance at 25 ℃	-50	–	+50	ppm
	Oscillation Mode	Fundamental			–
	Maximum change over temperature range	-50	–	+50	ppm
PON	Drive level	–	–	50	uW
CL	Equivalent Load capacitance	–		–	pF
CL1,CL2	Internal Load capacitance(CL1=CL2)	–		–	pF
RS	Series Resistance(ESR)	–		–	Ω
	Duty Cycle	30	50	70	%
CM	Motional capacitance	–	–		pF
CSHUT	Shunt capacitance	–	–		pF
RBIAS	Internal bias resistor				MΩ

Table 6-4 24MHz Oscillator Characteristics

6.5. Power up/down and Reset Specifications



The external voltage regulator and other power-on devices must provide the processor with a specific sequence of power and resets to ensure proper operation.

7. PWM

7.1. Overview

The output of the PWM is a toggling signal whose frequency and duty cycle can be modulated by its programmable registers. Each channel has a dedicated internal 16-bit up counter. If the counter reaches the value stored in the channel period register, it resets. At the beginning of a count period cycle, the PWMOUT is set to activate state and count from 0x0000.

The PWM divider divides the clock (24MHz) by 1-4096 according to the pre-scalar bits in the PWM control register.

In PWM cycle mode, the output will be a square waveform; the frequency is set to the period register. In PWM pulse mode, the output will be a positive pulse or a negative pulse.

7.2. PWM Signal Description

Signal Name	Description	Type	Pin Name	Ball#
PWM0	PWM output for port 0	O	PB2	K20
PWM1	PWM output for port 1	O	PG13	H3

Table 7. PWM Signal Description

8. Async Timer Controller

8.1. Overview

The chip implements 6 timers.

Timer 0/1/2 can take their inputs from the PLL6/6 or OSC24M. They provide the operating system's scheduler interrupt. It is designed to offer maximum accuracy and efficient management, even for systems with long or short response time. They provide 32-bit programmable overflow counter and work in auto-reload mode or no-reload mode.

The watch-dog is used to resume controller operation by generating a general reset or an interrupt request when it is disturbed by malfunctions such as noise sand system errors. It features a down counter that allows a watchdog period of up to 16 seconds.

Timer 3 is used for OS to generate a periodic interrupt.

9. Sync Timer Controller

9.1. Overview

The chip implements 2 sync timers for high-speed counter.

10. Interrupt Controller

10.1. Overview

The interrupt controller features:

- Control the nIRQ and FIQ of a RISC Processor
- Up to 96 interrupt sources
- 4-Level Priority Controller
- External Sources of Edge-sensitive or Level-sensitive

Since the 4-level Priority Controller allows users to define the priority of each interrupt source, so higher priority interrupts can be serviced even if a lower priority interrupt is being treated.

11. DMA Controller

11.1. Overview

There are two kinds of DMA in the chip. One is Normal DMA with 8 channels, and the other is Dedicated DMA with 8 channels.

For normal DMA, only one channel can be active and the sequence is in accordance with the priority level. As for the dedicated DMA, at most 8-channel can be active at the same time if their source or destination does not conflict.

12. SDRAM Controller

12.1. Overview

The SDRAM Controller (DRAMC) provides a simple, flexible, burst-optimized interface to all industy-standard double data rate II (DDR2) ordinary SDRAM and Double data rate III (DDR3) ordinary SDRAM. It supports up to a 16G bits memory address space.

The DRAMC automatically handles memory management, initialization, and refresh operations. It gives the host CPU a simple command interface, hiding details of the required address, page, and burst handling procedures. All memory parameters are runtime-configurable, including timing, memory setting, SDRAM type, and Extended-Mode-Register settings.

The DRAMC includes following features:

- Support DDR2 SDRAM and DDR3 SDRAM
- Support different memory device power voltage of 1.5V and 1.8V
- Support DDR2/3 SDRAM of clock frequency up to DDR1066
- Support memory capacity up to 16G bits (2G Bytes)
- Support 2 chip select signals
- 15 address lines and 3 bank address lines
- Data IO size can up to 32-bit for DDR2 and DDR3 (x8, x16)
- Automatically generate initialization and refresh sequences
- Runtime-configurable parameters setting for application flexibility
- Clock frequency can be chosen for different applications
- Priority of transferring through multiple ports is programmable
- Support random read or write operation

12.2. SDRAM Signal Description

Signal Name	Description	Type	Pin Name	Ball#

Signal Name	Description	Type	Pin Name	Ball#
SDQ0	SDRAM Data Bus bit0	I/O	SDQ0	K1
SDQ1	SDRAM Data Bus bit1	I/O	SDQ1	U2
SDQ2	SDRAM Data Bus bit2	I/O	SDQ2	J2
SDQ3	SDRAM Data Bus bit3	I/O	SDQ3	V1
SDQ4	SDRAM Data Bus bit4	I/O	SDQ4	J3
SDQ5	SDRAM Data Bus bit5	I/O	SDQ5	W1
SDQ6	SDRAM Data Bus bit6	I/O	SDQ6	J1
SDQ7	SDRAM Data Bus bit7	I/O	SDQ7	V2
SDQ8	SDRAM Data Bus bit8	I/O	SDQ8	T1
SDQ9	SDRAM Data Bus bit9	I/O	SDQ9	M1
SDQ10	SDRAM Data Bus bit10	I/O	SDQ10	U1
SDQ11	SDRAM Data Bus bit11	I/O	SDQ11	K2
SDQ12	SDRAM Data Bus bit12	I/O	SDQ12	R2
SDQ13	SDRAM Data Bus bit13	I/O	SDQ13	L1
SDQ14	SDRAM Data Bus bit14	I/O	SDQ14	T2
SDQ15	SDRAM Data Bus bit15	I/O	SDQ15	L2
SDQ16	SDRAM Data Bus bit16	I/O	SDQ16	W4
SDQ17	SDRAM Data Bus bit17	I/O	SDQ17	Y11
SDQ18	SDRAM Data Bus bit18	I/O	SDQ18	Y3
SDQ19	SDRAM Data Bus bit19	I/O	SDQ19	V12
SDQ20	SDRAM Data Bus bit20	I/O	SDQ20	Y2
SDQ21	SDRAM Data Bus bit21	I/O	SDQ21	W12
SDQ22	SDRAM Data Bus bit22	I/O	SDQ22	W2
SDQ23	SDRAM Data Bus bit23	I/O	SDQ23	Y12
SDQ24	SDRAM Data Bus bit24	I/O	SDQ24	Y8
SDQ25	SDRAM Data Bus bit25	I/O	SDQ25	W6
SDQ26	SDRAM Data Bus bit26	I/O	SDQ26	Y10

Signal Name	Description	Type	Pin Name	Ball#
SDQ27	SDRAM Data Bus bit27	I/O	SDQ27	Y4
SDQ28	SDRAM Data Bus bit28	I/O	SDQ28	W10
SDQ29	SDRAM Data Bus bit29	I/O	SDQ29	W5
SDQ30	SDRAM Data Bus bit30	I/O	SDQ30	W11
SDQ31	SDRAM Data Bus bit31	I/O	SDQ31	Y5
SDQS0	SDRAM Data Strobe 0	I/O	SDQS0	N1
SDQS0#	SDRAM Data Strobe 0 Invert	I/O	SDQS0#	N2
SDQM0	SDRAM Data Mask 0	O	SDQM0	P1
SVREF0	SDRAM Reference Input 0	AI	SVREF0	L4
SDQM1	SDRAM Data Mask 1	O	SDQM1	M2
SDQS1	SDRAM Data Strobe 1	I/O	SDQS1	P2
SDQS1#	SDRAM Data Strobe 1 Invert	I/O	SDQS1#	R1
SDQS2	SDRAM Data Strobe 2	I/O	SDQS2	W7
SDQS2#	SDRAM Data Strobe 2 Invert	I/O	SDQS2#	Y7
SDQM2	SDRAM Data Mask 2	O	SDQM2	W8
SVREF1	SDRAM Reference Input 1	AI	SVREF1	U11
SDQM3	SDRAM Data Mask 3	O	SDQM3	Y6
SDQS3	SDRAM Data Strobe 3	I/O	SDQS3	W9
SDQS3#	SDRAM Data Strobe 3 Invert	I/O	SDQS3#	Y9
SCK#	SDRAM Clock Invert	O	SCK#	Y1
SCK	SDRAM Clock	O	SCK	W2
SCKE0	SDRAM Clock Enable	O	SCKE0	L3
SCKE1	SDRAM Clock Enable	O	SCKE1	U5
SA0	SDRAM Data Address bit0	O	SA0	V7
SA1	SDRAM Data Address bit1	O	SA1	R4
SA2	SDRAM Data Address bit2	O	SA2	U8
SA3	SDRAM Data Address bit3	O	SA3	U7

Signal Name	Description	Type	Pin Name	Ball#
SA4	SDRAM Data Address bit4	O	SA4	P3
SA5	SDRAM Data Address bit5	O	SA5	V8
SA6	SDRAM Data Address bit6	O	SA6	R3
SA7	SDRAM Data Address bit7	O	SA7	V10
SA8	SDRAM Data Address bit8	O	SA8	T3
SA9	SDRAM Data Address bit9	O	SA9	V9
SA10	SDRAM Data Address bit10	O	SA10	M3
SA11	SDRAM Data Address bit11	O	SA11	T4
SA12	SDRAM Data Address bit12	O	SA12	P4
SA13	SDRAM Data Address bit13	O	SA13	U9
SA14	SDRAM Data Address bit14	O	SA14	U3
SWE	SDRAM Write Enable	O	SWE	V3
SCAS	SDRAM Column address strobe	O	SCAS	V4
SRAS	SDRAM Row address strobe	O	SRAS	U4
SCS0	SDRAM Chip Select 0	O	SCS0	V5
SCS1	SDRAM Chip Select 1	O	SCS1	N4
SBA0	SDRAM Bank Address 0	O	SBA0	U6
SBA1	SDRAM Bank Address 1	O	SBA1	N3
SBA2	SDRAM Bank Address 2	O	SBA2	V6
SODT0	SDRAM ODT Control Signal 0	O	SODT0	V11
SODT1	SDRAM ODT Control Signal 1	O	SODT1	M4
SRST	SDRAM Reset	O	SRST	U10
SZQ	SDRAM ZQ calibration	A	SZQ	K3
VDD_DLL	DLL Power Supply	P	VDD_DLL	J4/J5
GND_DLL	DLL Ground	G	GND_DLL	K4/K5

Table 12. SDRAM Signal Description

13. NAND Flash Controller

13.1. Overview

The NFC supports all NAND/MLC flash memory available in the market and new types can be supported by software re-configuration as well. There are 4 separate chip select lines (CE#) to connect up to 4 flash chips with 2 R/B signals.

The On-the-fly error correction code (ECC) is built in NFC to enhance reliability. BCH is implemented to detect and correct up to 64 bits error per 512 or 1024 bytes data. The on chip ECC and parity checking circuitry of NFC frees CPU for other tasks. The ECC function can be disabled by software.

The data can be transferred by DMA or by CPU memory-mapped IO method. The NFC provides automatic timing control to read or write external Flash. The NFC maintains the proper relativity for CLE, CE# and ALE control signal lines. Three kinds of modes are supported for serial read access: Mode 0 is the conventional serial access, Mode 1 for EDO type, and Mode 2 is for extension EDO type. In addition, NFC can monitor the status of R/B# signal line.

Block management and wear leveling management are implemented in software.

The NFC features:

- Support SLC/MLC/TLC flash and EF-NAND memory
- Software configure seed to randomize engine
- Software configure method for adaptability to a variety of system and memory types
- Support 8-bit Data Bus Width
- Support 1024, 2048, 4096, 8192, 16384 bytes size per page
- Up to 4 flash chips which are controlled by NFC_CEx#
- Support Conventional and EDO serial access method for serial reading Flash

- On-the-fly BCH error correction code which correcting up to 64 bits per 512 or 1024 bytes
- Corrected Error bits number information report
- NFC status information is reported by its registers and support interrupt
- One Command FIFO
- Support external DMA for data transfer
- Two 256x32-bit RAM for Pipeline Procession
- Support SDR, ONFI DDR and Toggle DDR NAND

13.2. NAND Flash Controller Signal Description

Signal Name	Description	Type
NCE[3:0]	NAND FLASH Chip Select bit	O
NRB[1:0]	NAND FLASH Chip Ready/Busy bit	I
NWE	NAND FLASH Chip Write Enable	O
NRE	NAND FLASH Chip Read Enable	O
NALE	NAND FLASH Chip Address Latch Enable	O
NCLE	NAND FLASH Chip Command Latch Enable	O
NWP	NAND FLASH Chip Write Protect	O
NDQ[7:0]	NAND FLASH Data bit	I/O
NDQS	NAND FLASH Data Strobe	I/O

Table 13. NAND Flash Controller Signal Description

14. SD/MMC Controller

14.1. SD/MMC Overview

The SD/MMC controller can be configured as a Secure Digital Multimedia Card controller, which simultaneously supports Secure Digital memory (SD Memo), UHS-1 Card, Secure Digital I/O (SDIO), Multimedia Cards (MMC), eMMC Card and Consumer Electronics Advanced Transport Architecture (CE-ATA).

The SD/MMC controller features:

- Support Secure Digital memory protocol commands (up to SD3.0)
- Support Secure Digital I/O protocol commands
- Support Multimedia Card protocol commands (up to MMC4.3)
- Support CE-ATA digital protocol commands
- Support eMMC boot operation and alternative boot operation
- Support Command Completion signal and interrupt to host processor and Command Completion Signal disable feature
- Support one SD (Verson1.0 to 3.0) or MMC (Verson3.3 to 4.3) or CE-ATA device
- Support hardware CRC generation and error detection
- Support programmable baud rate
- Support host pull-up control
- Support SDIO interrupts in 1-bit and 4-bit modes
- Support SDIO suspend and resume operation
- Support SDIO read wait
- Support block size of 1 to 65535 bytes

- Support descriptor-based internal DMA controller
- Internal 16x32-bit (64 bytes total) FIFO for data transfer

14.2. SD/MMC Controller Signal Description

SDCx=SDC[2:0]

Signal Name	Description	Type
SDCx_CLK	SDx/SDIOx/MMCx Clock signal	O
SDCx_CMD	SDx/SDIOx/MMCx Command Line	I/O
SDCx_D	SDx/SDIOx/MMCx Data bit	I/O

Table 14. SD/MMC Controller Signal Description

15. Two Wire Interface

15.1. Overview

This Two Wire Interface(TWI) Controller is an interface between CPU host and the serial 2-Wire bus, which supports all standard 2-Wire transfer, including Slave and Master. The communication to the 2-Wire bus is carried out on a byte-wise basis using interrupt or polled handshaking. This 2-Wire Controller can be operated in standard mode (100K bps) or fast-mode (up to 400K bps). Multiple Masters and 10-bit addressing Mode are supported for this specified application. General Call Addressing is supported in Slave mode.

The TWI Controller features:

- Software-programmable for Slave or Master
- Support Repeated START signal
- Support Multi-master systems
- Support 10-bit addressing with 2-Wire bus
- Perform arbitration and clock synchronization
- Own address and General Call address detection
- Support speed up to 400K bits/s (‘fast mode’)
- Support operation from a wide range of input clock frequencies

15.2. TWI Controller Signal Description

TWIx=TWI[2:0]

Signal Name	Description	Type
TWIx_SCK	TWI-BUS Clock for Channel x	I/O
TWIx_SDA	TWI-BUS Data for Channel x	I/O

Table 15. TWI Controller Signal Description

16. SPI Interface

16.1. Overview

The SPI is the Serial Peripheral Interface which allows rapid data communication with less software interrupts. The SPI module contains one 8x64 receiver buffer (RXFIFO) and one 8x64 transmit buffer (TXFIFO). It can work in two modes: Master mode and Slave mode.

It features:

- Full-duplex synchronous serial interface
- Configurable Master/Slave
- 8x64 FIFO for data transmit and receive
- Configurable Polarity and phase of the Chip Select (SPI_SS) and SPI Clock (SPI_SCLK)
- Support Dedicated DMA

16.2. SPI Controller Signal Description

SPIx=SPI[2:0]

Signal Name	Description	Type
SPIx_CS	SPIx Chip Select signal	I/O
SPIx_MOSI	SPIx Master data Out, Slave data In	I/O
SPIx_MISO	SPIx Master data In, Slave data Out	I/O
SPIx_CLK	SPIx Clock signal	I/O

Table 16. SPI Controller Signal Description

17. UART Interface

17.1. Overview

The UART is used for serial communication with a peripheral, modem (data carrier equipment, DCE) or data set. Data is written from a master (CPU) over the APB bus to the UART and it is converted to serial form and transmitted to the destination device. Serial data is also received by the UART and stored for the master (CPU) to read back.

The UART contains registers to control the character length, baud rate, parity generation/checking, and interrupt generation. Although there is only one interrupt output signal from the UART, there are several prioritized interrupt types responsible for its assertion. Each of the interrupt types can be separately enabled/disabled with the control registers.

The UART has 16450 and 16550 modes of operation, which are compatible with a range of standard software drivers. In 16550 mode, transmit and receive operations are both buffered by FIFOs. In 16450 mode, these FIFOs are disabled.

The UART supports word lengths from five to eight bits, an optional parity bit and 1, 1.5 or 2 stop bits, and is fully programmable by an AMBA APB CPU interface. A 16-bit programmable baud rate generator and an 8-bit scratch register are included, together with separate transmit and receive FIFOs. Eight modem control lines and a diagnostic loop-back mode are provided.

Interrupts can be generated for a range of TX Buffer/FIFO, RX Buffer/FIFO, Modem Status and Line Status conditions.

The UART includes the following features:

- Compatible with industry-standard 16550 UARTs
- 64-Bytes Transmit and receive data FIFOs
- DMA controller interface

- Software/ Hardware Flow Control
- Programmable Transmit Holding Register Empty interrupt
- Interrupt support for FIFOs, Status Change

17.2. UART Controller Signal Description

UARTx=[3:0]

Signal Name	Description	Type
UARTx_TX	UARTx Transmit Data	O
UARTx_RX	UARTx Receive Data	I
UARTx_CTS	UARTx Clear To Send	I
UARTx_RTS	UARTx Request To Send	O
UART1_RING	UARTx Ring Indicator	I
UART1_DTR	UARTx Data Terminal Ready	O
UART1_DSR	UARTx Data Set Ready	I
UART1_DCD	UARTx Data Carrier Detect	I

Table 17. UART Controller Signal Description

18. CIR Interface

18.1. Overview

The CIR features:

- Full physical layer implementation
- Support CIR for remote control or wireless keyboard
- 8x64-bit FIFO for data transfer
- Programmable FIFO thresholds
- Support Interrupt and DMA

CIR receiver is implemented in hardware to save CPU resource.It samples the input signals on the programble frequency and records these samples into RX FIFO when one CIR signal is found on the air. The CIR receiver uses Run-Length Code (RLC) to encode pulse width, and the encoded data is buffered in a 64 levels and 8-bit width RX FIFO: the MSB bit is used to record the polarity of the receiving CIR signal (The high level is represented as 1 and the low level is represented as 0), and the rest 7 bits are used for the length of RLC. The maximum length is 128. If the duration of one level (high or low) is more than 128, another byte is used. Since there are always some noises in the air, a threshold can be set to filter the noises to reduce system loading and improve system stability.

18.2. CIR Controller Signal Description

Signal Name	Description	Type
IR_TX	CIR Transmit Data	O
IR_RX	CIR Receive Data	I

Table 18. CIR Controller Signal Description

19. USB DRD Controller

19.1. Overview

The USB DRD is dual-role controller supporting Host and device functions. It can also be configured as a Host-only or Device-only controller, full compliant with the USB 2.0 Specification. The USB DRD can support high-speed (HS, 480-Mbps), full-speed (FS, 12-Mbps), and low-speed (LS, 1.5-Mbps) transfers in Host mode, support high-speed (HS, 480-Mbps) and full-speed (FS, 12-Mbps) in Device mode.

The USB2.0 DRD controller (SIE) features:

- 64-Byte Endpoint 0 for Control Transfer
- Support up to 5 User-Configurable Endpoints for Bulk , Isochronous**,** Control and Interrupt bi-directional transfers
- Support High-Bandwidth Isochronous & Interrupt transfers
- Support point-to-point and point-to-multipoint transfer in both Host and Peripheral mode

19.2. USB DRD Controller Signal Description

Signal Name	Description	Type
UDM0	USB0 DRD DM	AIO
UDP0	USB0 DRD DP	AIO

Table 19. USB DRD Controller Signal Description

20. USB Host Controller

20.1. Overview

USB Host Controller is fully compliant with the USB 2.0 specification, Enhanced Host Controller Interface (EHCI) Specification, Revision 1.0, and the Open Host Controller Interface (OHCI) Specification Release 1.0a. The controller supports high-speed, 480-Mbps transfers (40 times faster than USB 1.1 full-speed mode) using an EHCI Host Controller, as well as full and low speeds through one or more integrated OHCI Host Controllers.

It features:

- Include an internal DMA Controller for data transfer with memory.
- Comply with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0, and the Open Host Controller Interface (OHCI) Specification, Version 1.0a.
- Support High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps), and Low-Speed (LS, 1.5-Mbps) Device.
- Support only 1 USB Root Port shared between EHCI and OHCI

20.2. USB Host Controller Signal Description

Signal Name	Description	Type
DM1	USB1 HOST DM	AIO
DP1	USB1 HOST DP	AIO

Table 20. USB Host Controller Signal Description

21. Digital Audio Interface

21.1. Overview

The Digital Audio Interface can be configured as I2S interface or PCM interface by software. When configured as I2S interface ,it can support the industry standard format for I2S, left-justified, or right-justified. PCM is a standard method used to digital audio for transmission over digital communication channels. It supports linear 13 or 16-bit linear, or 8-bit u-law or A-law companded sample formats at 8K samples/s and can receive and transmit on any selection of four of the first four slots following PCM_SYNC.

It features:

- I2S or PCM configured by software
- Full-duplex synchronous serial interface
- Configurable Master / Slave Mode operation
- Audio data resolutions of 16, 20, 24
- I2S Audio data sample rate from 8Khz to 192Khz
- I2S Data format for standard I2S, Left Justified and Right Justified
- I2S supports 2 channel output and 2 channel input
- PCM supports linear sample (8-bit or 16-bit), 8-bit u-law and A-law companded sample
- One 128x24-bit FIFO for data transmit, one 64x24-bit FIFO for data receive
- Programmable FIFO thresholds
- Interrupt and DMA Support
- Two 32-bit Counters for AV sync application
- Loopback mode for test

21.2. Digital Audio Signal Description

Signal Name	Description	Type
I2S_MCLK	I2S Main Clock(system clock)	I/O

I2S_BCLK	I2S serial Bit Clock	I/O
I2S_LRCK	I2S Left or Right channel select clock(frame clock)	I/O
I2S_DO	I2S serial Data Output bit	O
I2S_DI	I2S serial Data Input	I

Table 21. Digital Audio Controller Signal Description

22. Ethernet MAC

22.1. Overview

The Ethernet MAC Controller enables the host to transmit and receive data over Ethernet in compliance to the IEEE 802.3-2002 standard. It supports 10M/100M external PHY with MII interface in both full and half duplex modes, and supports a 16K byte SRAM for continuous data transmission, flow control as well as DA/SA filtering.

The Ethernet MAC Controller (EMAC) features:

- Support 10/100Mbps data rate
- Support full and half duplex operations
- Support IEEE 802.3x flow control for full-duplex operation
- Support back-pressure flow control for half-duplex operation
- Support DA/SA Filtering
- Support Loop back operations
- Provide MII Interface for external Ethernet PHY
- 3K Bytes FIFO for TX
- 13K Bytes FIFO for RX

22.2. EMAC Signal Description

Signal Name	Description	Type
ERXD3	EMAC MII Receive Data Nibble Data Bit3	I
ERXD2	EMAC MII Receive Data Nibble Data Bit2	I
ERXD1	EMAC MII Receive Data Nibble Data Bit1	I
ERXD0	EMAC MII Receive Data Nibble Data Bit0	I
ETXD3	EMAC MII Transmit Data Nibble Data Bit3	O
ETXD2	EMAC MII Transmit Data Nibble Data Bit2	O
ETXD1	EMAC MII Transmit Data Nibble Data Bit1	O

Signal Name	Description	Type
ETXD0	EMAC MII Transmit Data Nibble Data Bit0	O
ERXCK	EMAC MII Receive Clock Input	I
ERXERR	EMAC MII Receive Error	I
ERXDV	EMAC MII Receive Data Valid	I
EMDC	EMAC MII Management Data Clock	O
EMDIO	EMAC MII Management Data Input/Output	I/O
ETXEN	EMAC MII Transmit Enable	O
ETXCK	EMAC MII Transmit Clock Input	I
ECRS	EMAC MII Carrier Sense	I
ECOL	MII Collision Detect	I
ETXERR	EMAC MII Transmit Error	O

Table 22. EMAC Signal Description

23. Transport Stream Controller

23.1. Overview

The transport stream controller is responsible for de-multiplexing and pre-processing the inputting multimedia data defined in ISO/IEC 13818-1. It receives multimedia data stream from SSI (Synchronous Serial Port)/SPI (Synchronous Parallel Port) inputs and de-multiplexs the data into Packets by PID (Packet Identify), and then the Packet will be stored to memory by DMA.The TS controller can be used for almost all multimedia applications, for example, DVB STB, IPTV, Streaming-media Box, multimedia players, etc.

The Transport Stream Controller features:

- One external Synchronous Parallel Interface (SPI) or one external Synchronous Serial Interface (SSI)
- 32 channels PID filter
- Support Multiple transport stream packet (188, 192, 204) format
- Configurable SPI and SSI timing parameters
- Hardware packet synchronous byte error detection
- Hardware PCR packet detection
- Configurable SPI transport stream generator for streams in DRAM memory
- Support DMA for data transfer

23.2. TS Signal Description

Signal Name	Description	Type
TS_CLK	TS System Clock	I
TS_ERR	TS Error Indicate Signal	I
TS_SYNC	TS Synchronization Control Signal	I
TS_DVLD	TS Valid Signal	I
TS_D[7:0]	TS Input Data Bit	I

Table 23. TS Signal Description

24. Audio Codec

24.1. Overview

The embedded Audio Codec is a high-quality stereo audio codec with headphone amplifier, which features:

- On-chip 24-bit DAC for play-back
- On-chip 24-bit ADC for recorder
- Support analog/ digital volume control
- Support 48K and 44.1K sample family
- DAC supports 192K and 96K sample
- Support FM/ Line-in/ Microphone recorder
- Stereo headphone amplifier that can be operated in capless headphone mode
- Support Virtual Ground to automatic change to True Ground to protect headphone amplifierand make function work normal mode

24.2. Audio Codec Signal Description

Signal Name	Description	Type
HPL	Headphone Left channel output	O
HPR	Headphone Right channel output	O
HPCOM	Headphone amplifier output	O
HPCOM_FB	Headphone amplifier Feedback	I
HPBP	Headphone Bypass output	O
FMINL	Audio ADC Input for Left Channel of FM Radio	I
FMINR	Audio ADC Input for Right Channel of FM Radio	I
MICIN1	MIC1 Input	I
MICIN2	MIC2 Input	I
MIC1OUTP	Micphone Positive Output	O
MIC1OUTN	Micphone Negative Output	O
LINEINL	Audio ADC Input for Left Channel of Line-in	I

LINEINR	Audio ADC Input for Right Channel of Line-in	I

Table 24. Audio Codec Signal Description

25. LRADC

25.1. Overview

LRADC is 6-bit resolution and can work up to maximum conversion rate of 250Hz.

It features:

- Support APB 32-bit bus width
- Support interrupt
- Support hold key and general key
- Support single key and continue key mode
- 6-bit resolution
- Voltage input range between 0 to 2V
- Sample Rate up to 250Hz

25.2. LRADC Signal Description

Signal Name	Description	Type
LRADC[1:0]	Low Resolution ADC input(6bit)	I

Table 25. LRADC Signal Description

26. Touch Panel Controller

26.1. Overview

The controller is a 4-wire resistive touch screen controller, includes 12-bit resolution A/D converter. Especially, it provides the ability of dual touch detection. The controller through the implementation of the two A/D conversion has been identified by the location of the screen of single touch, in addition to measurable increase in pressure on the touch screen.

It features:

- 12 bit SAR type A/D converter
- 4-wire I/F
- Dual Touch Detect
- Touch-pressure measurement (Support program set threshold)
- Sampling frequency: 2MHz (max)
- Single-ended conversion of touch screen inputs and ratiometric conversion of touch screen inputs
- TACQ up to 262ms
- Median and averaging filter to reduce noise
- Pen down detection, with programmable sensitivity
- Support X, Y change function

26.2. Touch Panel Signal Description

Signal Name	Description	Type
X[2:1]	Touch Panel ADC input	AI
Y[2:1]	Touch Panel ADC input	AI

Table 26. Touch Panel Signal Description

27. Keypad Interface

27.1. Overview

The Keypad Interface is used to connect external keypad devices, which provides up to 8 rows and 8 columns. The events of key press or key release can be detected to the CPU by an interrupt. To prevent switching noises, internal debouncing filter is provided.

The Keypad Interface features:

- Interrupt for key press or key release
- Internal debouncing filter to prevent the switching noises

27.2. Keypad Signal Description

Signal Name	Description	Type
KP_INx [7:0]	Keypad Interface RowX Data	I
KP_OUTx[7:0]	Keypad Interface ColumnX Data	O

Table 27. Keypad Signal Description

28. TV Encoder

28.1. Overview

The TV encoder enables the display of digital information on analog television sets as well as the new generation of standard digital televisions, providing a high quality, flicker-free viewing experience across the key global video standards NTSC and PAL.

28.2. TV-OUT Signal Description

Signal Name	Description	Type
TV_OUT	TV Analog Output	O

Table 28. TV-OUT Signal Description

29. Camera Sensor Interface

29.1. Overview

The CSI features:

- 8 bits input data
- Support CCIR656 protocol for NTSC and PAL
- 3 parallel data paths for image stream parsing
- Support Received data double buffer
- Parsing bayer data into planar R, G, B output to memory
- Parsing interlaced data into planar or MB Y, Cb, Cr output to memory
- Pass raw data direct to memory
- All data transmit timing can be adjusted by software
- Luminance statistical value

29.2. CSI Signal Description

Signal Name	Description	Type
CSI_PCLK	Camera Sensor Pixel Clock	I
CSI_MCLK	Camera Sensor Clock	O
CSI_HSYNC	Camera Sensor Horizontal Synchronization	I
CSI_VSYNC	Camera Sensor Verizontal Synchronization	I
CSI_D[7:0]	Camera Sensor Data Bit	I/O

Table 29. Camera sensor Signal Description

30. HDMI Controller

30.1. Overview

Basic Video/Audio Features:

- HDMI V1.4 compliance
- Support up to 165M pixel/second
- Support Max 4K*4K resolution
- Support 480I/576I/480P/576P/720P/1080I/1080P at 24/25/30/50/59.9hz
- Support 24/30/36/48-bit RGB data format, with 2X/4X repeater
- Support up to 8 channel , 24bit PCM(IEC60958)
- Support IEC61937 compress audio formats
- Support 1-bit audio
- Support HD audio (DTS-HD and Dolly MAT, IEC61937 format)
- Hardware Receiver active sense and Hot plug detect
- Interrupts for programmers

DDC Master Features:

- DDC Host Mode operation
- 7-bit addressing
- Arbitration lost and ACK error detection
- Support Slave clock extension
- Support Interrupt/DMA and polling transfer mode
- FIFO flow control by SCL holding
- 16-byte FIFO
- Max 1023-byte data transfer
- Implicit and Explicit offset address transfer
- Support E-DCC read

30.2. HDMI Signal Description

Signal Name	Description	Type
HHPD	HDMI Hot Plug Detection Signal	I/O
HSDA	HDMI Data	I/O
HSCL	HDMI Clock	I/O
HCEC	HDMI Consumer Electronic Control signal	I/O
HTXCP	TMDS Positive clock	I/O
HTXCN	TMDS Negative Clock	I/O
HTXxP [2:0]	TMDS positive data	I/O
HTXxN [2:0]	TMDS negative data	I/O

Table 30. HDMI Signal Description

31. Port Controller

31.1. Port Description

The chip has 7 ports for multi-functional input/out pins. They are:

- Port A(PA): 18 input/output port
- Port B(PB): 21input/output port
- Port C(PC): 20 input/output port
- Port D(PD): 28 input/output port
- Port E(PE): 12 input/output port
- Port F(PF): 6 input/output port
- Port G(PG): 14 input/output port

These ports can be easily configured by software for various system configurations. 32 external PIO interrupt sources are supported and interrupt mode can be configured by software.

32. Declaration

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